CLAIMS

[Claim(s)]
[Claim 1] A drive circuit of a capacitive load which is characterized by providing the following and which impresses a pulse of positive/negative amphipathy to a capacitive load which has the 1st and 2nd electrodes by turns A charge recovery circuit which delivers and receives a charge periodically between said 1st electrode The 1st clamping circuit which clamps said 1st electrode to the 1st or 2nd predetermined potential in some [at least] periods other than a period of transfer of said charge The 2nd clamping circuit which carries out floating of said 2nd electrode corresponding to a period of transfer of some said charges while clamping said 2nd electrode to the 3rd or 4th predetermined potential
[Claim 2] Said 1st predetermined potential and the 3rd predetermined potential are substantially equal, and said 2nd predetermined potential and the 4th predetermined potential are the equal drive circuit of a capacitive load according to claim 1 substantially.
[Claim 3] A drive circuit of a capacitive load according to claim 1 or 2 where said charge recovery circuit contains a capacitor for charge recovery, and a reactor.
[Claim 4] A drive circuit of a capacitive load according to claim 1 or 2 where said charge recovery circuit is constituted as a circuit using back EMF of a reactor.
[Claim 5] In a drive method of a capacitive load of impressing a pulse of positive/negative amphipathy to a capacitive load which has the 1st and 2nd electrodes by turns Maintaining a step and the 2nd electrode which collect charges from the 1st electrode and maintain the 1st electrode subsequently to the 1st potential, maintaining the 2nd electrode to one predetermined potential to one [said] predetermined potential Carrying out floating of a step and the 2nd electrode which return a charge to the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential Maintaining a step and the 2nd electrode which collect charges from the 1st electrode to predetermined potential of another side Maintaining a step and the 2nd electrode which return a charge to the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential to predetermined potential of said another side A drive method of a capacitive load characterized by having periodically [boil a step which returns a charge to the 1st electrode and maintains the 1st electrode subsequently to the 2nd potential one by one, carrying out floating of a step which collects charges from the 1st electrode, and the 2nd electrode, and].
[Claim 6] In a drive method of a capacitive load of impressing a pulse of positive/negative amphipathy to a capacitive load which has the 1st and 2nd electrodes by turns Maintaining a step and the 2nd electrode which give a charge to the 1st electrode and maintain the 1st electrode subsequently to the 1st potential, maintaining the 2nd electrode to one predetermined potential to said predetermined potential Carrying out floating of a step and the 2nd electrode which collect charges from the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential Maintaining a step and the 2nd electrode which give a charge to the 1st electrode to predetermined potential of another side Maintaining a step and the 2nd electrode which collect charges from the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential to predetermined potential of said another side A drive method of a capacitive load characterized by having periodically [boil a step which collects charges from the 1st electrode and maintains the 1st electrode subsequently to the 2nd potential one by one, carrying out floating of a step which gives a charge to the 1st electrode, and the 2nd electrode, and].
[Claim 7] A drive method of a capacitive load according to claim 5 or 6 characterized by said capacitive load being a flat display panel.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the drive circuit and method of a capacitive load of the charge recovery mold which can be especially manufactured by components mark smaller than before about the drive circuit and the drive method of a capacitive load.
[0002]
[Description of the Prior Art] As a capacitive load which needs the bipolar pulse of positive/negative, there are flat panels, such as the plasma display panel and electro luminescent panel which are used as image display devices, such as an information terminal equipment, and a personal computer or television, and a liquid crystal panel, etc. As a drive circuit of the conventional capacitive load, the drive circuit of a plasma display panel (PDP) is described here.
[0003] Drawing 9 is a cross section which meets the train electrode of one display cel of PDP. PDP is equipped with the 1st insulating substrate 11 of a glass front face, and the 2nd insulating substrate 12 on the back in this drawing. On the 1st insulating substrate 11, the 1st insulating layer 20 of a wrap and the 1st septum 21 of the shape of a grid which divides a display cel are formed one by one in the transparent scan electrode 17 and the transparent maintenance electrode 18 which constitute a line electrode, the bus electrode 19 formed on each [these] line electrode, and the whole electrode, and the protective layer 22 which covers the 1st insulating layer 20 and consists of MgO etc. further is formed.
[0004] On the 2nd insulating substrate 12, the 2nd septum 15 of the shape of the shape of a grid which divides a display cel in collaboration with the 2nd insulating layer 14 of a wrap and the 1st septum 15, and a stripe is formed one by one in the transparent train electrode (data electrode) 13 which intersects perpendicularly with a line electrode, and a train electrode, these whole is covered, and the fluorescent substance 16 is applied. The discharge gas space 23 which constitutes each display cel by the 1st and 2nd septa 21 and 15 is formed in the shape of a grid, and the discharge gas space 23 is filled up with discharge gas, such as rare gas.
[0005] Drawing 10 is a mimetic diagram shown in the electrode configuration paying attention to the whole above PDP. PDP25 has the structure where the 1st front insulating substrate 11 and the 2nd insulating substrate 12 on the back were ******(ed), and the seal of the building envelope is airtightly carried out by the seal section 26. On a drawing, each scan electrode 17 is a sign S1, and S2, ..., Sm, each maintenance electrode 18 is a sign C1, and C2, ..., Cm, and each train electrode 13 is shown by a sign D1, D2, ..., Dn-1, and Dn. In addition, in the following description, aij shows the display cel 24 of the intersection of the i-th line electrode and the j-th train electrode, for example.
[0006] Drawing 11 shows the wave of the driver voltage used by the drive of Above PDP. Setting to this drawing, wave (A) is the maintenance electrode C1, and C2, ..., Cm. The voltage waveform impressed Wave (B) is the scan electrode S1. The voltage waveform by which the voltage waveform impressed is impressed to wave (C) by the scan electrode S2 About the voltage waveform by which wave (D) is impressed to the scan electrode Sm, wave (E) is the train electrode D1. Wave (G) shows the luminescence wave of the display cel a11 for the voltage waveform by which the voltage waveform impressed is impressed to wave (F) by the train electrode D2, respectively. in addition, a wave -- (E) and a wave -- the slash pulse of the data pulses 34 shown by (F) shows that the existence of a pulse is determined according to the data which should be written in.
[0007] Hereafter, actuation of the conventional PDP of the above-mentioned form is explained briefly. In addition, the first transition of a pulse points out a pulse portion after, as for a pulse portion after impression of a pulse voltage starts until it reaches the abbreviation last voltage, and the trailing edge of a pulse, removal of a pulse voltage starts until a pulse voltage is removed nearly completely into this specification. For example, in a straight polarity pulse, a start portion is the first transition of a pulse, and a fall portion is the trailing edge. Moreover, in a negative polarity pulse, the fall portion of a pulse is first transition and the standup portion of a pulse is a trailing edge.
[0008] First, each scan electrode S1, and S2, ..., Sm By impressing the blanking pulses 35 of negative polarity all at once, the maintenance discharge till then is once eliminated. the next -- the priming pulse 36 of negative polarity with the big amplitude -- all the maintenance electrodes C1 and C2 and ... it is impressed by Cm and priming discharge which generates the priming particle which serves as a kind of discharge in the case of write-in discharge is performed all over a panel. Subsequently, they are each scan electrode S1, and S2, ..., Sm about the priming blanking pulse 37 with the small amplitude so that priming discharge may not lead to maintenance discharge as it is. It impresses all at once.
[0009] Then, it synchronizes with this pulse and they are each train electrodes D1 and D2, ..., Dn-1, and Dn at the same time

it enters at a write-in conducting period and impresses the scan pulse 33 to each scan electrode S1, and S2, ..., Sm line sequential. The data pulse 34 is impressed. A desired display cel is made to generate write-in discharge by these scan pulse 33 and the data pulse 34. In the example of drawing 11 , by the data voltage waveform (E) and (F), data is written in the display cels a11 and a22, and data is not written in the display cels a12 and a21, but the purport to which the writing according to data is carried out is shown about display cels other than these.

[0010] Termination of a write-in conducting period impresses the maintenance pulses 31 and 32 of negative polarity to each scan electrode and a maintenance electrode by turns, respectively. Between a scan electrode and a maintenance electrode, the alternation maintenance pulse from which polarity changes by turns is impressed by these maintenance pulses 31 and 32. By this alternation maintenance pulse, maintenance discharge occurs between the scan electrode 17 and the maintenance electrode 18 in the display cel 24 which had write-in discharge before, and the display according to data is performed. Display brightness is controlled by the count which impresses these maintenance pulses 31 and 32.

[0011]

[Problem(s) to be Solved by the Invention] By the drive circuit and method of PDP of the above-mentioned former, ** and discharge of the electrostatic capacity formed mainly between the scan electrode of the display cel section and a maintenance electrode whenever a maintenance pulse is impressed to a scan electrode and a maintenance electrode, respectively are performed. For this reason, there was a defect that the so-called consumption of the power for ** and discharge of this electrostatic capacity and reactive power was large, in addition to luminescence power required for a display originally.

[0012] In order to remove the above-mentioned defect, the charge recovery mold drive circuit which has the charge recovery circuit which collects the discharge charges of the electrostatic capacity in the case of each maintenance pulse impression is proposed (for example, a patent public presentation [Heisei 5] No. 265397, 63 years [of patent public presentation Showa] No. 101897). Here, drawing 11 , drawing 12 , and drawing 13 are collectively referred to supposing the case where the drive wave shown in drawing 11 is used, and the conventional charge recovery mold drive circuit is explained. Drawing 12 shows the drive circuit of the conventional PDP of this form as a block diagram, and drawing 13 shows each block of drawing 12 as a fundamental circuit diagram. At drawing 13 , the same reference mark showed the element corresponding to the element of drawing 12 .

[0013] In drawing 12 , the PDP drive circuit is prepared for the drive of PDP25 containing the display cel group 41 which has the scan electrode 17 and the maintenance electrode 18. A PDP drive circuit includes the priming pulse generating circuit 42 and charge recovery circuit which impress the priming pulse 36 to the maintenance electrode 18. The maintenance electrode side maintenance pulse generating circuit 43 which impresses the maintenance pulse 31 to the maintenance electrode 18, the elimination pulse generating circuit 44 which generates a blanking pulse 35 and the priming blanking pulse 37, the scan pulse generating circuit 45 which generates the scan pulse 33, and a charge recovery circuit are included. It has the mixing circuit 47 which impresses the scan electrode side maintenance pulse generating circuit 46 which generates the maintenance pulse 32 by the side of a scan electrode and the maintenance pulse 32 by the side of a scan electrode, the scan pulse 33, and blanking pulse 35 grade according to a package or an individual to each scan electrode 17 corresponding to the function.

[0014] In drawing 13 , the maintenance electrode side maintenance pulse generating circuit 43 consists of clamping circuit 43a and charge recovery circuit 43b, and the scan electrode side maintenance pulse generating circuit 46 consists of clamping circuit 46a and charge recovery circuit 46b similarly. Each clamping circuits 43a and 46a are constituted as a switching circuit which fixes a corresponding electrode to power supply potential-VS or touch-down (gland) potential periodically (clamp), and each charge recovery circuits 43b and 46b consist of the coils 101, 102, and 103 and the charge recovery capacitors 111 and 112 which constitute LC resonance circuit. Each charge recovery circuits 43b and 46b have the function to collect from these the charges accumulated in the corresponding scan electrode 17 or the corresponding maintenance electrode 18, and to return that charge to these, and hold down consumption of reactive power by this function.

[0015] As mentioned above, the charge recovery circuits 43b and 46b are again returned to the electrode which is prepared in each by the side of the maintenance electrode 18 and the scan electrode 17, and generally once collects the charges accumulated in these electrodes, and corresponds this charge. By the way, it consists of a switching circuit and LC resonance circuit, and circuitry is complicated, the manufacture costs also increase, and these charges recovery circuit has the defect of raising the cost of the whole drive circuit greatly.

[0016] Especially, in a maintenance electrode side, a voltage swing treats the high priming pulse 36. For this reason, it is necessary to use a high withstand voltage element also for charge recovery circuit 43b contained in the maintenance electrode side maintenance pulse generating circuit 43. Such a high withstand voltage element is expensive, and causes the further cost rise of a drive circuit.

[0017] The purpose of this invention is improving and having the drive circuit of the conventional capacitive load which has a charge recovery circuit, and adopting a simple configuration, and is to offer the drive circuit of the capacitive load which has a charge recovery circuit which can be manufactured by the low price.

[0018]

[Means for Solving the Problem] In a drive circuit of a capacitive load where a drive circuit of a capacitive load of this invention impresses a pulse of positive/negative amphipathy to a capacitive load which has the 1st and 2nd electrodes by turns in order to attain the above-mentioned purpose A charge recovery circuit which delivers and receives a charge periodically between said 1st electrode, The 1st clamping circuit which clamps said 1st electrode to the 1st or 2nd predetermined potential in some [at least] periods other than a period of transfer of said charge, While clamping said 2nd electrode to the 3rd or 4th predetermined potential, it is characterized by having the 2nd clamping circuit which carries out floating of said 2nd electrode

corresponding to a period of transfer of some said charges.
[0019] Moreover, a drive method of a capacitive load of this invention is set to a drive method of a capacitive load of impressing a pulse of positive/negative amphipathy to a capacitive load which has the 1st and 2nd electrodes by turns. Maintaining a step and the 2nd electrode which collect charges from the 1st electrode and maintain the 1st electrode subsequently to the 1st potential, maintaining the 2nd electrode to one predetermined potential to said predetermined potential Carrying out floating of a step and the 2nd electrode which return a charge to the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential Maintaining a step and the 2nd electrode which collect charges from the 1st electrode to predetermined potential of another side Maintaining a step and the 2nd electrode which return a charge to the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential to predetermined potential of said another side Carrying out floating of a step which collects charges from the 1st electrode, and the 2nd electrode, a step which returns a charge to the 1st electrode and maintains the 1st electrode subsequently to the 2nd potential is boiled one by one, and it is characterized by having periodically.
[0020] It replaces with above. A drive method of a plasma display panel of this invention In a drive method of a capacitive load of impressing a pulse of positive/negative amphipathy to a capacitive load which has the 1st and 2nd electrodes by turns Maintaining a step and the 2nd electrode which give a charge to the 1st electrode and maintain the 1st electrode subsequently to the 1st potential, maintaining the 2nd electrode to one predetermined potential to said predetermined potential Carrying out floating of a step and the 2nd electrode which collect charges from the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential Maintaining a step and the 2nd electrode which give a charge to the 1st electrode to predetermined potential of another side Maintaining a step and the 2nd electrode which collect charges from the 1st electrode and maintain the 1st electrode subsequently to the 2nd potential to predetermined potential of said another side Carrying out floating of a step which gives a charge to the 1st electrode, and the 2nd electrode, a step which collects charges from the 1st electrode and maintains the 1st electrode subsequently to the 2nd potential can be boiled one by one, and it can also constitute so that it may be characterized by having periodically.
[0021] There is especially no limit in a capacitive load driven by a drive circuit and a drive method of a capacitive load of this invention here, and each pulse of positive negative polarity should just be the capacitive load driven by alternation pulse which appears by turns. For example, plane panels, such as a plasma display panel, an electroluminescence panel (EL panel), and a liquid crystal panel, are mentioned.
[0022]
[Function] By the drive circuit and the drive method of a capacitive load of this invention In case the charges of the 1st electrode are collected and the potential of the 1st electrode is reduced, floating of the 2nd electrode is carried out. The 2nd electrode is made to follow potential fluctuation of the 1st electrode using the 1st electrode and the 2nd inter-electrode capacity coupling. In case similarly a charge is returned to the 1st electrode and the potential of the 1st electrode is started, floating of the 2nd electrode can be carried out, and the 2nd electrode can be made to follow potential fluctuation of the 1st electrode. Desired potential fluctuation can be given to the 2nd electrode without establishing a charge recovery circuit in a 2nd electrode side by combining immobilization of the potential of the 2nd electrode, and flattery of the potential fluctuation by floating by request here.
[0023]
[Example] Hereafter, with reference to a drawing, this invention is further explained to details based on the suitable example of this invention. Here, as a capacitive load driven in the drive circuit of the capacitive load of this invention, a plasma display panel (PDP) is explained as an example like the conventional example. Drawing 1 is the block diagram of the drive circuit of the capacitive load of one example of this invention. Moreover, drawing 2 shows each block of drawing 1 as a basic circuit diagram. The maintenance electrode side maintenance pulse generating circuit consists of drive circuits of the capacitive load of this example only in the clamping circuit excluding the charge recovery circuit. Other block configurations are the same as the block configuration of the conventional drive circuit.
[0024] The maintenance electrode clamping circuit 1 where the drive circuit of this example generates the maintenance pulse for the maintenance electrode 18 in drawing 1 , The priming pulse generating circuit 42 which generates the priming pulse for the maintenance electrode 18, The scan pulse generating circuit 45 which generates a scan pulse, and the scan electrode maintenance pulse generating circuit 46 which generates the maintenance pulse for a scan electrode, It consists of an elimination pulse generating circuit 44 which generates the blanking pulse and priming blanking pulse for a scan electrode, and a mixing circuit 47 which gives a scan pulse, a maintenance pulse, a blanking pulse, etc. to each scan electrode 17 according to a package or an individual.
[0025] In drawing 2 , the output of the maintenance electrode clamping circuit 1 has the switches 159 and 158 for connecting with the maintenance electrode 18 connected in common, and fixing a maintenance electrode to -VS potential or ground potential periodically, or making it floating. As for the priming pulse generating circuit 42, peak value gives the priming pulse of -VP to the maintenance electrode 18.
[0026] A mixing circuit 47 is equipped with one pair of diodes, 121 and 123, which are arranged every scan electrode 17 and connected mutually at a serial, and 122 and 124, and the connection node which connects one pair each of diodes mutually is connected to each scan electrode 17, respectively. [for example,] By this configuration, it functions as a mixing circuit 47 giving a scan pulse, a blanking pulse, a priming blanking pulse, and the maintenance pulse by the side of a scan electrode individually to each scan electrode 17 for every class of that at a package.
[0027] The scan pulse generating circuit 45 has one pair of switches, 151 and 153, arranged every scan electrode 17, and 152

and 154, and the connection node of one pair each of switches is connected to each scan electrode 17 which corresponds via a mixing circuit 47, respectively. [for example,] Peak value the elimination pulse generating circuit 44 - The priming blanking pulse or peak value of VPE generates the blanking pulse of -VE, and these are given to the scan electrode 17 via a mixing circuit 47 at a package. The scan electrode maintenance pulse generating circuit 46 has the function to collect the charges of the scan electrode 17 at the time of the maintenance pulse supply while it consists of scan electrode clamping circuit 46a and charge recovery circuit 46b and supplies a maintenance pulse to the scan electrode 17 via a mixing circuit 47.
[0028] Drawing 3 is the timing chart showing actuation of one period in drawing 1 and the maintenance pulse impression period in PDP of drawing 2 . this drawing -- setting -- a wave -- the maintenance pulse train by which 51 is impressed to the scan electrode 17 -- a wave -- 52 shows the maintenance pulse train impressed to the maintenance electrode 18, respectively. moreover, a wave -- 53 is the voltage difference of the scan electrode 17 and the maintenance electrode 18, and shows the alternation maintenance pulse train which is impressed to the discharge space of each display cel, and functions effectively because of charge maintenance. ON of each switch and the timing of OFF are further shown in drawing 3 , and reference marks 60-72 show each actuation period in one period in a maintenance conducting period to it.
[0029] During a maintenance conducting period, since, as for each switches 151-157 in the scan pulse generating circuit 45, the priming pulse generating circuit 42, and the elimination pulse generating circuit 44, there is no direct relation to generating and impression of this maintenance pulse, they are maintained at an off condition by each.
[0030] First, in the period 60, the switch 158 of the maintenance electrode clamping circuit 1 is set to ON, therefore, as for the scan electrode 17 and the maintenance electrode 18, the switch 160 of ON and scan electrode clamping circuit 46a is all clamped for it by ground potential. Moreover, the potential of the charge recovery capacitor 111 in charge recovery circuit 46b is in abbreviation-VS potential at this time.
[0031] In a period 61, the switch 163 of OFF and charge recovery circuit 46b is set to ON for the switch 160 of scan electrode clamping circuit 46a as [** / which set the switch 158 of the maintenance electrode clamping circuit 1 to ON]. Thereby, via one diode of the coil 102 in charge recovery circuit 46b, diode 126, and one pair each of diodes of a mixing circuit 47, 123 and 124, the charges of the scan electrode 17 are collected to the charge recovery capacitor 111, and the potential of a scan electrode is reduced even in -VS neighborhood by LC resonance. [for example,] At this time, the terminal voltage of the charge recovery capacitor 111 starts to ground potential to near.
[0032] In a period 62, the switch 161 in OFF and scan electrode clamping circuit 46a is again set to ON for the switch 163 in charge recovery circuit 46b, and the potential of the scan electrode 17 is clamped to the potential of -VS. In a period 63, the switch 162 in OFF and charge recovery circuit 46b is set to ON for a switch 161, the charge of the charge recovery capacitor 111 is returned to the scan electrode 17 side via the diode, 121 and 122, of another side of the coil 101 in charge recovery circuit 46b, diode 125, and a pair each of diode in a mixing circuit 47, and the potential of the scan electrode 17 is again started to the ground potential neighborhood. [for example,] At this time, the potential of the charge recovery capacitor 111 falls even to -VS neighborhood mostly.
[0033] In a period 64, the switch 160 of OFF and scan electrode clamping circuit 46a is set to ON for a switch 162, and the potential of the scan electrode 17 is clamped to ground potential. The actuation from the above-mentioned period 60 to a period 64 is the same as the actuation in the charge recovery mold drive circuit of the conventional capacitive load. Here, the maintenance pulse 54 of the negative polarity which has first transition and a trailing edge at periods 61 and 63, respectively is impressed to the scan electrode 17 before periods 61-63.
[0034] Then, in a period 65, the switch 158 in ON and the maintenance electrode clamping circuit 1 is made [the switch 160 in scan electrode clamping circuit 46a] off for the switch 163 of OFF and charge recovery circuit 46b. By ON of a switch 163, the charges of the scan electrode 17 are collected by the charge recovery capacitor 111, and the potential of the scan electrode 17 falls even to -VS neighborhood mostly. Since the switches 157, 158, and 159 which have led to the maintenance electrode 18 at this time are OFF altogether, a maintenance electrode is in floating and the potential of the maintenance electrode 18 is followed by capacity coupling of the maintenance electrode 18 and the scan electrode 17 at the potential of the scan electrode 17.
[0035] In a period 66, the switch 159 of OFF and the maintenance electrode clamping circuit 1 is set to ON for a switch 163, and the potential of the maintenance electrode 18 is clamped to -VS. Subsequently, in a period 67, the potential of the scan electrode 17 is mostly started even in the ground potential neighborhood by setting the switch 162 of charge recovery circuit 46b to ON, and returning a charge from the charge recovery capacitor 111. As shown in wave 51 from a period 65 to the above period 67, the maintenance pulse 57 of the negative polarity which has first transition and a trailing edge at periods 65 and 67 is impressed to the scan electrode 17. subsequently, a switch 162 is turned OFF in a period 68 -- the scan electrode 17 is both clamped to ground potential by setting the switch 160 of scan electrode clamping circuit 46a to ON.
[0036] In a period 69, the switch 163 of OFF and charge recovery circuit 46b is set to ON for the switch 160 of scan electrode clamping circuit 46a, charges are collected to the charge recovery capacitor 111, and the potential of the scan electrode 17 is again reduced even in -VS neighborhood. Since the switch 159 of the maintenance electrode clamping circuit 1 is set to ON like the above at this time, the potential of the maintenance electrode 18 is fixed to -VS.
[0037] Subsequently, a switch 163 is made off in a period 70. In a period 71, the switch 159 of the maintenance electrode clamping circuit 1 is further made off in this condition. The switch 162 of charge recovery circuit 46b is set to ON, a charge is returned to the scan electrode 17 side from the charge recovery capacitor 111, and the voltage of the scan electrode 17 is mostly started even to ground potential at coincidence. since all the switches that lead to the maintenance electrode 18 are OFF states at this time -- the maintenance electrode 18 -- floating -- it is -- capacity coupling of the maintenance electrode 18

and the scan electrode 17 -- the potential of the maintenance electrode 18 -- the potential of the scan electrode 17 -- following -- this -- ** -- it starts in parallel. As shown in wave 51 from a period 69 to the above period 71, the maintenance pulse 58 of the negative polarity which has first transition and a trailing edge at periods 69 and 71, respectively is impressed to the scan electrode 17.

[0038] Subsequently, in a period 72, the scan electrode 17 and the maintenance electrode 18 are clamped to ground potential, respectively by setting the switch 160 of scan electrode clamping circuit 46a, and the switch 158 of a maintenance electrode clamping circuit to ON. As shown in the maintenance electrode 18 in wave 52 from the above period 65 before a period 72, the maintenance pulse 56 of the negative polarity which has first transition and a trailing edge, respectively is impressed to periods 65 and 72.

[0039] It will set by the above-mentioned periods 60-72. Between the scan electrode 17 and the maintenance electrode 18 The pulse 55 of the negative polarity obtained with the maintenance pulse 54 of negative polarity and the ground potential of the maintenance electrode 18 which are impressed to the scan electrode 17 as seen in wave 53, The pulse 59 of the straight polarity by the ground potential between the maintenance pulses 57 and 58 of the scan electrode 17 and the negative potential level in the maintenance pulse 56 impression period of the negative polarity of the maintenance electrode 18 is impressed. That is, the alternation maintenance pulse which contributes to maintenance discharge is impressed to the discharge space between the scan electrode 17 in the display cel group 41, and the maintenance electrode 18.

[0040] By repeating periodically the drive actuation which makes one period from the above period 60 to the period 72, repeat impression of the alternation maintenance pulse can be carried out at the display cel group 41. Therefore, a capacitive load can be driven by charge recovery mold drive, without establishing a charge recovery circuit in a maintenance electrode side by using the drive circuit of the above-mentioned example. Thereby, the cost cut by the simplification of a circuit and improvement in the reliability accompanying reduction of the number of elements are realizable.

[0041] In addition, in the configuration of the above-mentioned example, the configuration which replaces with return of the charge to the charge recovery from a scan electrode and a scan electrode, and performs grant and recovery from these of the charge to a scan electrode, respectively is also employable. In this case, in the period 60 of the beginning of one period, a scan electrode and a maintenance electrode are maintained to -VS, respectively, and let potential of a charge recovery capacitor be an abbreviation grand level. Hereafter, it replaces with recovery of said charge, grant of a charge is replaced with return of a charge, and charges are collected. Also in this case, the same effect as the above-mentioned example is acquired.

[0042] Moreover, in description of the above-mentioned example, although explained with reference to the basic circuit of drawing 2 , the above-mentioned circuit is easily realizable using the present electronics technology. The case where the above-mentioned switch is realized by the field-effect transistor (it outlines Following FET) is illustrated to drawing 4 . In this drawing, reference mark 151F to 158F and 160F to 163F show FET corresponding to 158 and 160 to 163 from the switch 151 of drawing 2 , respectively.

[0043] Although the circuit of drawing 4 has the substantial almost same circuitry as the circuit of drawing 2 , in drawing 4 , FET group 159F which function as a bidirectional switch which consists of P channel FET (159FP) and N channel FET (159FN) are prepared corresponding to the switch 159 of drawing 2 . This prevents that the maintenance electrode 18 sways greatly in the minus direction further from peak value-VS in a period 69.

[0044] Generally, it is known for FET that parasitism diode will be formed in juxtaposition at the portion which functions as a switch. For example, as shown in drawing 5 , in P channel FET91, the parasitism diode 94 goes [the parasitism diode 92] into juxtaposition at N channel FET93. In order to prevent the short-circuit current resulting from these parasitism diodes 92 and 94, diodes 129-134 are formed in drawing 4 .

[0045] Peak value-VP of the priming pulse 36 impressed to a maintenance electrode as shown in drawing 11 as an example considers the larger case in the negative direction of being general than peak value-VS of the maintenance pulse 31. When diode 132 was not formed in the maintenance electrode clamping circuit 1 and FET (157F) of the priming pulse generating circuit 42 is set to ON in order to generate the priming pulse 36, it is -VS power supply Rhine. A short-circuit current will flow to ->FET(159FN) -> diode 131 ->FET(157F) ->-VP power supply Rhine. Other diodes which are not shown are formed in drawing 2 for the same purpose.

[0046] In addition, the above-mentioned example described as an example the case where the maintenance pulse of negative polarity was impressed to the scan electrode 17 and the maintenance electrode 18. However, the drive circuit of this invention can be applied, the scan electrode 17, when reaching and impressing the maintenance pulse of straight polarity to the maintenance electrode 18, respectively, and not only this but when. Drawing 6 is the basic circuit diagram of the drive circuit of the 2nd example showing this case. Corresponding to the coils 101 and 102 in drawing 2 , the charge recovery capacitor 111, diodes 121-126, and each of switches 151-153, coils 201 and 202, the charge recovery capacitor 211, diodes 221-226, and switches 251-263 are arranged. Since it is the same as that of the case of drawing 2 about a base of operation, detailed explanation is omitted.

[0047] In addition, as for the electrostatic capacity of the charge recovery capacitors 111 and 211, in each above-mentioned example, it is desirable to set up beyond the sum total of the electrostatic capacity of the display cel section 41 of PDP which constitutes a load. Moreover, the reactance of a coil takes into consideration the working speed of PDP, and LC resonance frequency of a circuit, and is determined.

[0048] Drawing 7 is drawing showing the configuration of the 3rd example of this invention with drawing 2 similarly. Unlike the configuration of charge recovery circuit 46b of drawing 2 , in this example, the configuration of other configurations of charge recovery circuit 46c is the same as that of drawing 2 . In addition, an example similar to the charge recovery circuit

shown in drawing 7 is seen by the patent public notice common No. 81912 [five to] official report. Drawing 8 is the timing chart showing similarly the actuation and the driver voltage wave of each switch in drawing 7 with drawing 3 .
[0049] Although not shown in drawing 8 , since, as for during the period which is impressing the maintenance pulse, there was no direct relation to generating and impression of a maintenance pulse, it has kept switches 151-157 each to the OFF state like the 1st example.
[0050] In a period 60, the switch 160 of ON and scan electrode clamping circuit 46a is also ON, and the scan electrode 17 and the maintenance electrode 18 are all clamped for the switch 158 of the maintenance electrode clamping circuit 1 by ground potential.
[0051] In a period 61, the switch 160 of scan electrode clamping circuit 46a is made off, setting the switch 158 of the maintenance electrode clamping circuit 1 to ON. Moreover, once set the switch 167 of charge recovery circuit 46c to ON, -VS power supply Rhine is made to flow through the scan electrode 17 via each diodes 123 and 124 of the coil 105 of charge recovery circuit 46c, and a mixing circuit 47, and the potential of the scan electrode 17 is reduced. a switch 167 is turned OFF when the potential of the scan electrode 17 becomes or less -VS/2 (between -VS/2 - -VS and the following -- the same). At this time, each diode 123 of the scan electrode 17 -> mixing circuit 47 and a 124 -> coil 105 -> diode 138 -> gland, and the current from the scan electrode 17 flow continuously according to an operation of back EMF generated in a coil 105. Thus, current is passed until the scan electrode 17 serves as potential of -VS, reducing the power loss of a circuit. Diode 137 has the function to return the power with which the coil 105 remained to -VS power supply Rhine, in cooperation with diode 138 while preventing the voltage by the side of the cathode of diode 137 becoming below -VS.
[0052] In a period 62, the switch 161 in scan electrode clamping circuit 46a is set to ON, and the voltage of the scan electrode 17 is clamped to -VS. Subsequently, in a period 63, once set the switch 166 of OFF and charge recovery circuit 46c to ON for a switch 161, a gland is made to flow through the scan electrode 17, and the potential of a scan electrode is started. A switch 166 is turned OFF when the potential of the scan electrode 17 becomes or more -VS/2. According to an operation of back EMF generated in a coil 104, the current of each diode 121 of the -VS power supply -> diode 136 -> coil 104 -> mixing circuit 47 and the 122 -> scan electrode 17, and a scan electrode flows continuously. Thus, the scan electrode 17 is started to ground potential, reducing the power loss of a circuit. Diode 135 has the function to return the power with which the coil 104 remained to -VS power supply, in cooperation with diode 136 while preventing the potential by the side of the anode of diode 135 becoming more than ground potential.
[0053] In a period 64, the potential of the scan electrode 17 is clamped to ground potential by setting the switch 160 in scan electrode clamping circuit 46a to ON. The maintenance pulse 84 is impressed to the scan electrode 17 between a period 61 and a period 63. The base of the actuation from a period 60 to a period 64 is the same as that of the circuit actuation shown in a patent public notice common 5-81912. Next, based on this invention, the portion which impresses a maintenance pulse to the maintenance electrode 18 by charge recovery circuit 46c is explained.
[0054] First, in a period 65, the switch 158 of OFF and the maintenance electrode clamping circuit 1 is made off for a switch 160, and the potential of the scan electrode 17 is once reduced in the negative direction by setting the switch 167 of charge recovery circuit 46c to ON. The actuation of charge recovery circuit 46c at this time itself is the same as the actuation in a period 61, and it will make a switch 167 off by the time of termination of a period 65. however -- since the switches 157, 158, and 159 which lead to the maintenance electrode 18 are altogether made into the OFF state in the period 65 -- a maintenance electrode -- floating -- it is -- a wave -- as shown in 82, the potential of the maintenance electrode 18 also follows the potential of the scan electrode 17, and is reduced.
[0055] In a period 66, the potential of the maintenance electrode 18 is clamped to -VS by setting the switch 159 of the maintenance electrode clamping circuit 1 to ON. Subsequently, in a period 67, the switch 166 of charge recovery circuit 46c is once set to ON, the voltage of the scan electrode 17 is started in the grand level direction, and a switch 166 is made off before termination of a period 67. The scan electrode 17 starts to ground potential within a period 67 according to an operation of back EMF of a coil. during a period 65 to the above period 67 -- setting -- a wave -- as shown in 81, the maintenance pulse 87 is impressed to the scan electrode 17. Then, in a period 68, the potential of the scan electrode 17 is clamped to ground potential by setting the switch 160 of scan electrode clamping circuit 46a to ON.
[0056] In a period 69, the switch 167 of OFF and charge recovery circuit 46c is once set to ON for the switch 160 of scan electrode clamping circuit 46a, and the potential of the scan electrode 17 is again reduced in the negative direction. Since the switch 159 of the maintenance electrode clamping circuit 1 is set to ON at this time, the potential of a maintenance electrode is clamped by -VS. When the potential of the scan electrode 17 amounts to or less -VS/2, a switch 167 is turned OFF like the case of a period 61.
[0057] In a period 70, the switch 159 of the maintenance electrode clamping circuit 1 is still ON. A switch 159 is made off in the next period 71, and all the switches that lead to the maintenance electrode 18 are made into an OFF state. With this, the potential of the scan electrode 17 is once started in the grand level direction by setting the switch 166 of charge recovery circuit 46c to ON. Since the maintenance electrode 18 is in floating at this time, the potential of the maintenance electrode 18 also follows the potential of the scan electrode 17, and is started. When the potential of the scan electrode 17 amounts to or more -VS/2, a switch 166 is made off like a period 63. during a period 69 to the above period 71 -- setting -- a wave -- as shown in 81, the maintenance pulse 88 is impressed to the scan electrode 17.
[0058] In a period 72, the scan electrode 17 and the maintenance electrode 18 are clamped to ground potential, respectively by setting the switch 160 of scan electrode clamping circuit 46a, and the switch 158 of the maintenance electrode clamping circuit 1 to ON. By actuation from the above period 65 to a period 72, the maintenance pulse 86 is impressed to the

maintenance electrode 18.
[0059] By the above-mentioned actuation, the voltage pulse impressed between a scan electrode and a maintenance electrode turns into the pulse 85 of the negative polarity by periods 61-63, and the pulse 89 of the straight polarity by periods 67-69, and the alternation pulse 83 is impressed between a scan electrode and a maintenance electrode like the 1st example.
[0060] In a maintenance conducting period, repeat impression of the alternation maintenance pulse 83 can be carried out at the display cel group 41 by repeating periodically the actuation which makes one period from the period 60 to the period 72. Therefore, also in the 3rd example, the charge recovery mold drive of a capacitive load is attained, without establishing a charge recovery circuit in a maintenance electrode side.
[0061] Each above-mentioned example described the drive circuit and the drive method of a capacitive load of this invention by making into an example the case where PDP of form explained with reference to drawing 9 and drawing 10 is driven. However, this invention is applicable not only to the drive of PDP of this form but the drive of the AC mold PDP of other form. Moreover, it is employable suitable not only for PDP but plane panels, such as other capacitive display panels, for example, an electro luminescent panel, and a liquid crystal panel. Furthermore, generally, this invention is applicable to the drive of any capacitive loads, if impression of the pulse of positive/negative amphipathy is a required capacitive load.
[0062] In the configuration of each above-mentioned example, although explained based on the suitable mode of this invention, correction and modification of versatility [configuration / of the above-mentioned example] are possible. For example, although the practical use circuit of drawing 4 showed the example which adopted FET as a switch, it can replace with FET and a bipolar transistor etc. can be adopted. Moreover, it can also constitute so that it may replace with a scan electrode side and a charge recovery circuit may be established in a maintenance electrode side. In addition, in this case, by PDP, it may originate in the operating voltage by the side of a maintenance electrode being high, and the cost of passive circuit elements may go up as compared with the case of an example. Furthermore, although each above-mentioned example described the case where a charge recovery circuit was used for all the periods of the first transition of a maintenance pulse, and a trailing edge, it replaces with this and you may make it use the charge recovery circuit in this invention for a part of first transition of a maintenance pulse, and/or trailing edge.
[0063]
[Effect of the Invention] Since the generating circuit of the alternation pulse impressed to a capacitive load is realizable by simple circuitry according to the drive circuit and the drive method of a capacitive load of this invention as explained above, this invention does so the remarkable effect which held down low the cost of the charge recovery mold drive circuit of a capacitive load, and raised circuit reliability.

[Translation done.]

[0022] (1) If switching-means 123B and 1261A-126nB are turned ON in this state, charges will be collected from the scanning electrodes Y1-Yn through coil 124B and switching-means 123B by the capacitor 122 for recovery. By inductance operation of coil 124B, even if the voltage of the scanning electrodes Y1-Yn is set to Vs/2, current continues flowing, and the voltage of the scanning electrodes Y1-Yn goes to GND level. However, the voltage of the scanning electrodes Y1-Yn has not fallen to GND level by the power consumption of the resistance component of this current path. Then, the current on which switch control-means 126B flows coil 124B at this time detects a bird clapper to 0, it flows through switching-means 125B slowly, and the charge which is set to 0 and in which the scanning electrodes Y1-Yn remained is made to discharge to a grand line side through switching-means 125B in this side for a while. At this time, it is completed as 0 by the voltage between terminals of switching-means 123B and coil 124B. And when it is thought that the scanning electrode Y1 was set to GND level, both switching-means 123B and switching-means 125B are turned OFF. In addition, it may not be simultaneous when turning OFF switching-means 123B and switching-means 125B.
[0023] After turning ON switching means 115, writing in the voltage of the maintenance electrode X at the time of control of (2) and (1) and making it go up to voltage Vw at it, switching means 115 are turned OFF. By this, the maintenance electrode X writes in from the maintenance electrode Vs, and it starts suddenly to voltage Vw, and writes in between the maintenance electrode X and the scanning electrodes Y1-Yn, and electric discharge arises.
(3) Next, turn ON simultaneously switching-means 112B and switching-means 123A. Thereby, the charges on the maintenance electrode X are collected through a coil 113 and switching-means 112B by the capacitor 111 for recovery, and the recovery charge of the capacitor 122 for recovery is simultaneously charged by the scanning electrodes Y1-Yn through switching-means 123A, coil 124A, and diode 1261B-126nB.
[0024] And switching-means 123B is closed. Moreover, the EMI effect can be decreased when the current which flows coil 124A detects a bird clapper to 0, switch control-means 126A operates so that switching-means 125A may be closed by around the time of the flow of current amounting to 0, and flyback current occurs. Moreover, turn ON switching-means 114B and the charge which remained on the maintenance electrode X which cannot be collected by the power consumption of the resistance component of a current path is made to discharge to a grand line side, and switching-means 125A is turned ON and, simultaneously with this, it is completed as 0 (the potential of each terminal is Vs) by the voltage between terminals of coil 124A (before maintenance electric discharge generating). When it is thought that the maintenance electrode X was set to GND level, and the scanning electrodes Y1-Yn became a sustaining voltage Vs, both switching-means 112B, switching-means 114B, switching-means 123A, and switching-means 125A are turned OFF. in addition, it may not be simultaneous when turning OFF the time of turning OFF switching-means 123A, and switching-means 125A (the following -- the same)
[0025] (4) Next, turn ON switching-means 112A. Thereby, the charge of the capacitor 111 for recovery is charged by the maintenance electrode X through switching-means 112A and a coil 113. at this time, the current on which the switch control means 116 flow a coil 113 detects a bird clapper to 0, and is set to 0 -- it flows through switching-means 114A slowly for a while in this side, and a charge is supplied to the maintenance electrode X through switching-means 114A from the sustaining-voltage supply line Vs And when it is thought that the maintenance electrode X became a sustaining voltage Vs, both switching-means 112A and switching-means 114A are turned OFF.
[0026] A) an address period -- in this period, the X driver 11 is not used but the maintenance electrode X is maintained at the sustaining voltage Vs Moreover, charge recovery / reuse circuit by the side of the Y driver 12 is not used, either. There is comparatively little useless power consumption in this period.
(5) Turn OFF switching-means 341B after turning ON only switching-means 341B and making voltage of the scanning electrode Y1 into GND level. The writing of an indicative data is performed to the 1st display line by address driver which is in this state, for example, is indicated by drawing 5 of JP,5-265397,A. That is, self-elimination electric discharge is performed between the address electrodes and the scanning electrodes Y1 corresponding to the cell which the 1st display line tends to switch off. Next, after turning ON only switching-means 341A and returning the voltage of the scanning electrode Y1 to a sustaining voltage Vs, switching-means 341A is turned OFF.
[0027] Hereafter, same operation is performed in this order about the 2nd - n display line.
S) Turn ON maintenance conducting period (6), next switching-means 112B. Thereby, the charges on the maintenance electrode X are collected through a coil 113 and switching-means 112B by the capacitor 111 for recovery. For a while, the current on which the switch control means 116 flow a coil 113 at this time is detected, and the charge which remained on the maintenance electrode X from which the current concerned is set to 0, and which flows through switching-means 114B slowly in this side, and cannot be collected is made to discharge to a grand line side, and when it is thought that the maintenance electrode X was set to GND level, both switching-means 112B and switching-means 114B are turned OFF.
[0028] (7) Next, turn ON switching-means 112A. Thereby, the recovery charge of the capacitor 111 for recovery is charged by the maintenance electrode X through switching-means 112A and a coil 113. at this time, the switch control means 116 detect the current which flows a coil 113, and the current concerned is set to 0 -- it flows through switching-means 114A slowly for a while in this side, and a charge is supplied to the maintenance electrode X through switching-means 114A from a sustaining voltage Vs And when it is thought that the maintenance electrode X became a sustaining voltage Vs, both switching-means 112A and switching-means 114A are turned OFF.
[0029] (8) Next, turn ON switching-means 123B and 1261B-126nB. Thereby, charges are collected from the scanning electrodes Y1-Yn through coil 124B and switching-means 123B by the capacitor 122 for recovery. The EMI effect can be decreased when the current which flows coil 124B detects a bird clapper to 0, switch control-means 126B operates so that

switching-means 125B may be slowly closed by around the time of the flow of current amounting to 0, and flyback current occurs in the meantime. Next, the charge which remained on the scanning electrode Y1 - Yn is made to discharge to a grand line side through switching-means 125B, turning ON switching-means 125B. And when it is thought that the scanning electrode Y1 was set to GND level, switching-means 123B and switching-means 125B are turned OFF.
[0030] (9) Next, turn ON switching-means 123A. Thereby, the recovery charge of the capacitor 122 for recovery is charged by the scanning electrodes Y1-Yn through switching-means 123A, coil 124A, and diode 1261A-126nA. The current on which switch control-means 126A flows coil 124A at this time detects a bird clapper to 0, and the EMI effect can be decreased, when [to which the flow of current amounts to 0] it flows through switching-means 125A and switching-means 123B slowly for a while in a front hit and flyback current occurs.
[0031] And a charge is supplied to the scanning electrodes Y1-Yn through switching-means 125A turned ON and diode 1261A-126nA from the maintenance electric discharge supply line Vs. And when it is thought that the scanning electrodes Y1-Yn became a sustaining voltage Vs, both switching-means 123A and switching-means 125A are turned OFF. Hereafter, operation of above-mentioned (6) - (9) is repeated.
[0032] In addition, timing which flows through the switching means 114A, 114B, 125A, and 125B mentioned above slowly is taken as the time of output voltage becoming 1/2 or more [of the maximum level] at the time of elevation, or the time or subsequent ones of output voltage becoming 1/2 or less [of the minimum level] at the time of descent. The switching means (switching-means 114B [as opposed to / switching-means 114A / For example,]) which correspond depending on the state of fault if output voltage makes it flow through switching means in 1/2 or less stage of the maximum level at the time of elevation are also because bird clappers are a **** and risk simultaneously at ON. Moreover, it is because a power efficiency is not good in this case, either.
[0033] As mentioned above, in this example, in the circuit which can collect and reuse the charge about charge and discharge also not only in the X driver 11 but in the Y driver 12 with easy composition, when generating of flyback current can be pressed down and flyback current occurs, the EMI effect is decreased. That is, ringing current is removable. In addition, the drive circuit in this example is constituted by a panel and one, and can be used for a plasma display as shown in drawing 10 which is panel display. Furthermore, you may use the panel display for a TV apparatus equipped with a broadcast receive section. By using for a TV apparatus, generating of a noise is pressed down and a flicker of a screen etc. can be reduced. In addition, the TV apparatus which equipped drawing 11 with the broadcast receive section is shown. Moreover, you may use panel display for the computer apparatus which has the processing unit which consists of alter operation equipment, CPUs, etc., such as a keyboard and a mouse. By using the plasma display concerned for a computer apparatus, a noise can be reduced and the effect that possibility that a malfunction will occur decreases arises. The example of a computer apparatus is shown in drawing 12 .
[0034] Moreover, diode as shown in drawing 13 is sufficient as switching-means 1261A-126nA and 1261B-126nB, and which switching means as shown in the views a, b, and 1 c of JP,7-109542,B are sufficient as them.
(Example 2) Next, the example 2 of this invention is explained with reference to drawing 3 .
[0035] Drawing 3 is drawing showing the concrete circuitry of an example 2, and consists of a reactive power recovery circuit 31 and one output circuit 32 of a driver IC. The reactive power recovery circuit 31 The capacitor 3101 for recovery The switching means 3107 and the end of a coil 3104 which connect the high potential side power supply 3105 with the switching means 3102 and switching means 3103 by which parallel connection was carried out, a coil 3104, the high potential side power supply 3105, the low voltage side power supply 3106, and the end of a coil 3104, and the low voltage side power supply 3106 It consisted of a low voltage side power supply 3110 connected with the switching means 3108 and the switch control means 3109 to connect, and the end of the capacitor 3101 for recovery, and is connected with one output circuit 32 of a driver IC through the output 3111 of a reactive power recovery circuit. Moreover, one output circuit 32 of a driver IC consists of an input terminal 3201, switching means 3202 and 3203, high potential side power terminals 3204 of a driver IC, and low voltage side power terminals 3205, and one output circuit 32 of a driver IC is connected to load-carrying capacity 34 from the output terminal 33. In addition, the switch control means 3109 detect the current which flows a coil 3104, and control each switching means by the current.
[0036] In this circuitry, if an input terminal 3201 is controlled and switching means 3202 are turned ON, the output pulse made in the reactive power recovery circuit 31 will be impressed to the electrode of an X-Y-matrix panel. Although capacitance exists in the electrode of a panel, the power accompanying charge and discharge is collected by the reactive power recovery circuit 31. If switching means 3203 are turned ON, an output is fixable to a low. and while collecting charges to the capacitor 3101 for recovery, the switch control means 3109 decide to detect the current which flows a coil 3104, it detects that the current was set to 0, and the flow of current amounts to 0 -- it flows through switching means 3105 slowly for a while in a front hit The EMI effect can be decreased when flyback current occurs by carrying out this control.
[0037] In addition, the timing which flows through the switching means 3107 and 3108 mentioned above slowly is the same as that of operation of a drive circuit which explained in the example 1, and is taken as the time of output voltage becoming 1/2 or more [of the maximum level] at the time of a rise, or the time or subsequent ones of output voltage becoming 1/2 or less [of the minimum level] at the time of descent. The switching means (switching means [as opposed to / switching means 3107 / For example,] 3108) which correspond depending on the state of fault if output voltage makes it flow through switching means in 1/2 or less stage of the maximum level at the time of a rise are also because bird clappers are a **** and risk simultaneously at ON. Moreover, it is because a power efficiency is not good in this case, either.
[0038] As mentioned above, according to this example, in the circuit in which charge recovery is possible, when flyback

current occurs, the EMI effect can be decreased. In addition, the drive circuit in this example is constituted by a panel and one, and can be used for a plasma display as shown in drawing 10 which is panel display. Furthermore, you may use the panel display for a TV apparatus equipped with a broadcast receive section. By using for a TV apparatus, generating of a noise is pressed down and a flicker of a screen etc. can be reduced. In addition, the TV apparatus which equipped drawing 11 with the broadcast receive section is shown. Moreover, you may use panel display for the computer apparatus which has the processing unit which consists of alter operation equipment, CPUs, etc., such as a keyboard and a mouse. By using the plasma display concerned for a computer apparatus, a noise can be reduced and the effect that possibility that a malfunction will occur decreases arises. The example of a computer apparatus is shown in drawing 12 .

[0039] (Example 3) Next, the example 3 of this invention is explained with reference to drawing 4 and drawing 5 . Drawing 4 shows the drive circuit of the plasma display of an example 3. The drive circuit shown in drawing 4 follows the proper voltage impressed to the electrodes 401 and 402 concerned. It is the plasma display which has the memory which can accumulate the charge of the specified quantity, and the electroluminescence function. And in order that the period of a series of display actions displayed on this display may choose two or more cell sections concerned and may perform write-in operation of a proper indicative data, The period which writes an indicative data in the cell section which performs the scan which chooses two or more display lines in line sequential, In the address period S-1 and this address period S-1, the cell section in which this indicative data was written For example, a predetermined period, In the display constituted so that you may make it constitute from a period S-2 which carries out a multiple-times electroluminescence, for example, a maintenance conducting period To each of two power supply lines FVH and FLG which while constitutes two or more this display lines scanned, and are connected to the driver circuit which makes an electrode 402, for example, Y electrode, drive While forming in parallel the driver circuit 400 which consisted of two switching means 403 and 404 Voltage predetermined to at least one side of each power supply line linked to the driver circuit concerned, At least between the 1st state, it operates so that switching means 403 may be in an open state. namely, a power circuit means 410 to impress the 1st power supply line and the switching means 420 to which the predetermined voltage impressed to each power supply line linked to this driver circuit is made to leak -- The signal drawn from a coil 405 is answered after that, and in order [to which the flow of the current of a coil 405 amounts to 0] to cheat to switch-on completely out of a few in a front hit, the switch control means 406 which operate so that switching means 413 may be closed slowly are formed.

[0040] This plasma display concerning this invention performs the display drive of a picture using the X electrode 401, the Y electrode 402, and three electrodes that consist of an address electrode which is not illustrated. That is, it sets in the drive circuit of the plasma display concerning this invention. As opposed to the scanning electrode 402 concerned Y electrode scan driver circuit group 4101 and 4102...410n which consisted of driver circuits which while connects with a driver circuit and give ON voltage (for example, GND) required in order to perform a scan, and OFF voltage (for example, Vsc) to a power supply line (1st power supply line), It is the voltage for a scan at this scanning driver circuit group 4101 and a power supply line common to 4102...410n. this -- with the power circuit means 410 installed in order to supply or intercept the voltage (it is Vsc at the voltage of OFF for example, at the time of a scan) of the 1st power supply means The voltage for this scan impressed to this scanning driver circuit group 4101 and each 4102...410n power supply line is made to leak, and the switching means 420 for setting voltage of this power supply line to 0V or GND are formed.

[0041] Furthermore, the power circuit means 410 in this example In the scanning address period S-1 which is a period which writes an indicative data in the cell section On the other hand, of the two power supply lines FVH and FLG linked to the driver circuit concerned, at least For example, 1st power supply means 410A which makes predetermined voltage, for example, Vsc, impress to FVH1 - FVHn (1st power supply line), Suppose that it consists of the 2nd power supply means 410B which makes predetermined voltage impress to FVH1 concerned - FVHn in the maintenance conducting period S-2 which is a period for predetermined carrying out period electric discharge of the cell section in which the indicative data was written.

[0042] furthermore, it is used in this invention -- this -- 1st power supply means 410A A high-voltage power supply, for example, the 1st voltage generating means 411 and low-battery power supply which generate Vsc, for example, it constitutes from the 2nd voltage generating means 412 to generate GND -- having -- this -- the 1st power supply generating means 411 one power supply line of the two power supply lines (FVH, FLG) linked to the aforementioned driver circuit -- for example it connects with Wiring FVH (1st power supply line) -- having -- this -- the 2nd voltage generating means 412 presupposes that it connects with the power supply line FLG (2nd power supply line), for example, wiring, of another side of the two power supply lines (FVH, FLG) linked to the aforementioned driver circuit

[0043] Switching means 413 and 414 are formed in each of said power supply meanses 411 and 412 used in this invention, respectively, and suppose that it is constituted so that wiring [which / of two power supply lines (FVH1 - FVHn, and FLG1 - FLGn) which connect predetermined voltage to a driver circuit with the predetermined control signal inputted from the outside] (for example, FVH1 - FVHn) may be supplied.

[0044] Furthermore, suppose that the above-mentioned switching means 413 and 414 consist of MOSFETs. furthermore, 1st power supply means 410A in the drive circuit of the display concerning this invention -- this -- suppose that diode, resistance, or its both are connected between one wiring of the two power supply lines linked to the 1st voltage generating means 411 and this driver circuit, for example, FVH, (1st power supply line)

[0045] on the other hand, the power circuit 410 used in the driving gear of the display in this invention is constituted -- this -- 2nd power supply means 410B consists of voltage generating meanses 415 and 416 to generate different potential of two pieces, and each voltage generating meanses 415 and 416 presuppose that the power supply line display line (FVH, FLG)

linked to a driver circuit is alike, respectively, and it connects individually
[0046] In this example, 2nd voltage generating means 416 by which connect with the power supply line FVH between two power supply lines linked to a driver circuit, and the 1st voltage generating means 415 which supplies GND potential supplies Vs which is a high voltage is connected to other power supply lines FLG (2nd power supply line) between two power supply lines linked to this driver circuit.
[0047] Furthermore, suppose that it is constituted so that it may supply for any of the power supply line (for example, FVH or FLG) which switching means 417 and 418 are formed, gets down, is inputted into voltage generating meanses 415 and 416 to constitute said 2nd power circuit 410B in this invention, from the outside, respectively, and connects predetermined voltage to this driver circuit with a predetermined control signal being.
[0048] Furthermore, the above-mentioned switching means 417 and 418 presuppose that it consists of MOSFETs. in addition, it described above -- this -- diode D410A and D410B may be connected to parallel at the MOSFET concerned which are the switching means 417 and 418 prepared in each voltage generating meanses 415 and 416 in 2nd power supply means 410B, respectively On the other hand, suppose at each switching means 413 and 414 of the scanning driver circuit by the side of Y electrode that diodes D407 and D408 are connected to parallel, respectively in the drive circuit of the display concerning this invention.
[0049] Moreover, the power supply line linked to the driver circuit by the side of Y electrodes each currently used in this invention is constituted between two power supply lines (FVH, FLG), and connection insertion of the driver circuit 4101 concerned is carried out in parallel with the power supply line (FVH, FLG) of these two books. In addition, it is a common electrode as described above, the electrode, i.e., X electrode, of another side in this display.
[0050] Moreover, the aforementioned leak control switch means 420 used in this invention may have the switching means 421 which consist of MOSFETs, and is connected to the power supply line (FVH) of the side to which the voltage generating means 411 of the above 1st is connected. next, each power supply line (FVH, FLG) which constitutes two power supply lines linked to this driver circuit in the display concerning this invention -- respectively -- being alike -- suppose that the charge recovery circuit 450 is connected
[0051] The charge recovery circuit 450 concerned presupposes that it consists of series resonant circuits with the capacity which a display panel has, and the coils 405 and 451 through diodes D407 and D408. In this invention, it is also possible to set up so that the inductance values of each coils 405 and 451 in the series resonant circuit 450 with this panel capacity constituted by the two sequences concerned and the coil through diode may differ mutually.
[0052] That is, from the peak voltage which generates this charge recovery way at the time of the resonance, it has two L-C resonance paths which consist of diode connected to this, or an MOSFET, and this charge recovery circuit 450 concerning this invention can be clamped to predetermined voltage (Vs or GND), it is stored in the capacitor which carries out the postscript of some of the charges, and uses the charge for the following scanning interval.
[0053] Said 2nd power circuit 410B has a switch function for supplying the current in the case of the maintenance conducting period which repeats display luminescence. In addition, although it is not limited and especially the detailed circuitry of this charge recovery circuit 450 can use a well-known charge recovery circuit conventionally In the example of drawing 1 , diodes D451, D452, D453, D454, D455, D456, D457, and D458 and switches 452 and 453, and also the capacitor 454 are using what consisted of arrays like illustration for everything but coils 405 and 451.
[0054] Although proper drive operation is performed in the drive circuit of the display concerning the above-mentioned this invention on the assumption that the above-mentioned composition While preparing the driver circuit which the fundamental composition of the drive method constituted this cell in the display which has said composition, and was constituted from two transistors by each of one electrode among the electrodes of the couple which discharges The 1st power supply means which makes predetermined voltage impress to each electrode concerned in the period which writes an indicative data in the aforementioned cell section, The 2nd power supply means which makes predetermined voltage impress to each electrode concerned in the period for predetermined carrying out period electric discharge of this cell section in which this indicative data was written, In the display on which the leak control switch means to which the predetermined voltage impressed to each electrode of this is made to leak is established Just before writing an indicative data in this cell section, the 1st power supply means concerned is operated. Just before the end of the period which writes an indicative data for predetermined voltage in the electrode concerned at impression ** bundle ****** and this cell section Stop the operation of the 1st power supply means and this leak control switch means is operated. the period for predetermined carrying out period electric discharge of the process which extinguishes the potential difference during wiring of the electrode concerned, and this cell section -- setting -- this -- it is the drive method which consists of processes which the 2nd power supply means is operated and are impressed to a police box electrode
[0055] Moreover, the potential difference of the both ends of this driver circuit 4101 in the period S-2 for predetermined carrying out period electric discharge of this cell section in which this indicative data was written as other modes of the drive method of this display concerning this invention, i.e., a maintenance conducting period, is maintained to 0, and display processing can be performed. Furthermore, diodes D407 and D408 are connected to each switches 403 and 404 of the driver circuit 4101 concerned at parallel, respectively, and you may make it the maintenance discharge voltage in the maintenance conducting period S-2 concerned make it impressed by the display panel through these diodes D407 and D408 from the 2nd power supply means 410B concerned.
[0056] Furthermore, an output as shown in drawing 5 is obtained by switch control as specifically shows the drive method of the driving gear in this example to drawing 5 . In the switch control shown in drawing 5 , the switch control means 406 and

455 detect the current which flows coils 405 and 451, respectively, and perform control from which the current concerned is set to 0 and which is a front hit for a while and closes switches 411 and 414 slowly, and when they amount to 0, it carries out switch-on completely.
[0057] Timing which begins to make it flow through switches 411 and 414 is similarly taken as the time of output voltage becoming 1/2 or more [of the maximum level] at the time of a rise, or the time or subsequent ones of output voltage becoming 1/2 or less [of the minimum level] at the time of descent with examples 1 and 2 having described. As mentioned above, according to this example, in the circuit in which charge recovery is possible, when flyback current occurs, the EMI effect can be decreased.
[0058] In addition, the drive circuit in this example is constituted by a panel and one, and can be used for a plasma display as shown in drawing 10 which is panel display. Furthermore, you may use the panel display for a TV apparatus equipped with a broadcast receive section. By using for a TV apparatus, generating of a noise is pressed down and a flicker of a screen etc. can be reduced. In addition, the TV apparatus which equipped drawing 11 with the broadcast receive section is shown. Moreover, you may use panel display for the computer apparatus which has the processing unit which consists of alter operation equipment, CPUs, etc., such as a keyboard and a mouse. By using the plasma display concerned for a computer apparatus, a noise can be reduced and the effect that possibility that a malfunction will occur decreases arises. The example of a computer apparatus is shown in drawing 12 .
[0059] (Example 4) Next, the example 4 of this invention is explained with reference to drawing 6 and drawing 7 . Drawing 6 shows the drive circuit of the plasma display of an example 4. IC of a high withstand voltage in which 601 drives a train electrode as for the drive circuit shown in drawing 6 , The terminal with which 602 impresses the direct current voltage for charge recovery of the abbreviation 1/2 for the data voltage Vd, The direct-current-voltage terminal of the data voltage Vd and 604 603 The earth terminal of IC (601), The train electrode from which it is set diode by 605, 606, and 607 and 608 is set as the object of charge recovery, And the capacitor for recovery which has electrostatic capacity with an abbreviation [for the compound electrostatic capacity of an auxiliary capacitor] of 100 or more times, The auxiliary capacitor for 609 making recovery **** small, the coil for charge recovery in 610, The switch control means which detect the current to which 611, 612, and 613 flow to switching means, and 614 flows in a coil, and control opening and closing of switching means by the value of the current, the terminal with which 615 connects a drive circuit with IC (601), and 616 are the terminals of 1 of a data electrode.
[0060] The voltage in the circuit which starts the 4th example of this invention at drawing 7 , a current wave form, etc. are shown. In a period T11, switching means 611 flow, it lets a coil 610, diode 607, and switching means 611 pass, and the charges currently stored in the auxiliary capacitor 609 are collected to the capacitor 608 for recovery. At the time of the end of a period T11, the voltage waveform of a terminal 603 serves as the minimum value near zero. In addition, during this period (T11), even when ON of switching means 612 is also off, they are not cared about. The dashed line of drawing 7 (D) shows this.
[0061] In a period T12, ON of the switching means which are not illustrated in IC (601) and OFF changes are performed. During this period (T12), even when ON of switching means 611 is also off, they are not cared about. The dashed line of drawing 7 (B) shows this. In a period T13, switching means 612 flow and the auxiliary capacitor 609 is charged through diode 606 and a coil 610. Moreover, in parallel to this, a charge is charged by each train electrode through the switching means as which the ON state is chosen for the inside's of switching means 612, diode 606, a coil 610, and IC (601) corresponding to existence of data and which are not illustrated, and a data pulse is formed. Since it charges through a coil 610, the power losses in a circuit are few. The voltage of a terminal 603 rises to near the data voltage Vd.
[0062] some of times of the current on which the switch control means 614 flow a coil being set to 0 at this time -- a front -- detecting -- the -- it begins to flow through switching means 613 slowly for a while at the last time Here, the timing which begins to flow through a switch 613 slowly is after the time of the voltage of the terminal 616 which is output voltage being 1/2 or more [of maximum]. It is because possibility that a power efficiency will become bad and a circuit will short-circuit by fault arises when the voltage of a terminal 616 is 1/2 or less [of maximum].
[0063] In a period T14, switching means 613 are in the state of ON with previous statement. Moreover, the voltage of a terminal 603 is clamped on the data voltage Vd. Moreover, the voltage value of each train electrode is fixed to voltage Vd by the switching means which are not illustrated in IC (601) according to the switching means 613 of an ON state, and the existence of data, and it is fixed to null voltage by the switching means in IC (601). In addition, during this period, even when ON of switching means 612 is also off, they are not cared about. The dashed line of drawing 7 (D) shows this.
[0064] Charge recovery of a data pulse and the writing of data are performed by the above operation. Moreover, the EMI effect is decreased, when generating of flyback current is pressed down and flyback current occurs by performing switch control which it begins to flow through switching means 613 slowly from a last time for a while when reduction of current which flows a coil by the switch control means 614 is detected and it is set to 0. That is, ringing current is removable.
[0065] In addition, the drive circuit in this example is constituted by a panel and one, and can be used for a plasma display as shown in drawing 10 which is panel display. Furthermore, you may use the panel display for a TV apparatus equipped with a broadcast receive section. By using for a TV apparatus, generating of a noise is pressed down and a flicker of a screen etc. can be reduced. In addition, the TV apparatus which equipped drawing 11 with the broadcast receive section is shown. Moreover, you may use panel display for the computer apparatus which has the processing unit which consists of alter operation equipment, CPUs, etc., such as a keyboard and a mouse. By using the plasma display concerned for a computer apparatus, a noise can be reduced and the effect that possibility that a malfunction will occur decreases arises. The example of

a computer apparatus is shown in drawing 12 .
[0066] (Example 5) Next, the example 5 of this invention is explained with reference to drawing 8 and drawing 9 . Drawing 8 shows the drive circuit of the plasma display of an example 5. IC of a high withstand voltage in which 801 drives a train electrode as for the drive circuit shown in drawing 8 , The terminal with which 802 impresses the direct current voltage for charge recovery of the abbreviation 1/2 for the data voltage Vd, The terminal for [803] charge recovery of IC (801) in the direct-current-voltage terminal of the data voltage Vd, and 804, The terminal into which 805 inputs the earth terminal of IC (801) into, and 806 inputs the data voltage Vd of IC (801), The train electrode from which it is set as the object for [83 / D / D81-] charge recovery in diode and 807, And the capacitor for charge recovery which has electrostatic capacity with an abbreviation [for the compound electrostatic capacity of an auxiliary capacitor] of 100 or more times, The auxiliary capacitor for 808 making small the rate of change of the recovery electrostatic capacity by change of the electrostatic capacity of the train electrode which should be collected, One of the output terminals of IC (801) by which the coil for charge recovery in 809, and 810, 811, 812, 813 and 814 are connected to switching means, and 815 is connected to each train electrode, and DP81 and DN81 are diodes. 816 is switch control means which perform control slowly flowed through switching means 812 for a while in a front hit when the current which flows a coil 809 is detected and the current concerned is set to 0.
[0067] In addition, much 815 illustrates one of the output terminals connected to one of the existing train electrodes. The voltage waveform in the circuit which starts the 5th example of this invention at drawing 9 etc. is shown. In a period T91, the voltage of the terminal 815 connected to the train electrode which a data pulse is not impressed before a period T91, but should newly impress a data pulse after a period T91 is pulled up, as shown in drawing 9 (F).
[0068] For this reason, it is made to flow through switching means 811, and the charge currently stored in the recovery capacitor 807 is charged at a train electrode through switching means 811, diode D82, a coil 809, switching means 812, and a terminal 815. And it is got blocked, and when the current which charge of the train electrode concerned completes and which flows a coil 809 is set to 0, the switch control means 816 begin to flow through switching means 814 slowly for a while in this side. In addition, the switch control means 816 detect the current which flows a coil 809, judge that it is this side a few at the time of the current concerned being set to 0, and begin to flow through switching means 814. The timing which flows through these switching means 814 is a time of output voltage, i.e., the voltage of a terminal 815, being 1 / after two of the maximum level like ****. According to the experiment, the time of about 75% of the maximum level of output voltage (voltage of a terminal 815) has the viewpoint of energy efficiency and EMI prevention to desirably good convenience.
[0069] In a period T92, since the switching means 813 in IC (801) are made off and the switching means 814 in IC (801) are succeedingly set to ON, a data pulse voltage is clamped on the data voltage Vd. In addition, in order that switching means 813 and 814 may carry out operation which conflicts mutually, when switching means 813 are ON (or OFF), switching means 814 are OFF (or ON).
[0070] In a period T93, since the following data pulse exists, the pulse voltage of a terminal 815 does not change. For this reason, in switching means 812, switching means 814 consider switching means 813 as as [of an OFF state] with an ON state with an OFF state. Since the voltage of a terminal 815 is still the data voltage Vd also in a period T94, the state of switching means 812, 814, and 815 is not changed.
[0071] In a period T95, the data pulse is impressed before the period T95, and the voltage of the terminal 815 connected with the train electrode which newly removes a data pulse after a period T95 is reduced (drawing 9 (F)). For this reason, it is made to flow through switching means 812, and the charges currently stored in the train electrode are collected to the capacitor 807 for recovery through a terminal 815, switching means 812, a coil 809, diode D83, and switching means 810.
[0072] And the time of finishing collecting to the capacitor 807 for recovery, i.e., when the current which flows a coil 809 is set to 0, begins to flow through switching means 813 slowly in front for a while. In addition, it detects that it is a front a few at the time of the current on which the switch control means 816 flow a coil 809 being set to 0, and the above switching means 813 are controlled.
[0073] thus, in this example, in the data pulse driver circuit which can heighten the laborsaving effect of a data pulse remarkably, and can realize high-speed operation, when generating of flyback current can be pressed down and flyback current occurs, decrease little of the EMI effect is carried out That is, ringing current is removable. In addition, the drive circuit in this example is constituted by a panel and one, and can be used for a plasma display as shown in drawing 10 which is panel display. Furthermore, you may use the panel display for a TV apparatus equipped with a broadcast receive section. By using for a TV apparatus, generating of a noise is pressed down and a flicker of a screen etc. can be reduced. In addition, the TV apparatus which equipped drawing 11 with the broadcast receive section is shown. Moreover, you may use panel display for the computer apparatus which has the processing unit which consists of alter operation equipment, CPUs, etc., such as a keyboard and a mouse. By using the plasma display concerned for a computer apparatus, a noise can be reduced and the effect that possibility that a malfunction will occur decreases arises. The example of a computer apparatus is shown in drawing 12 .

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The important section circuitry view of X driver in the example 1 of this invention, and Y driver
[Drawing 2] The voltage-waveform view showing one example of the drive method of the plasma display panel in the example 1 of this invention
[Drawing 3] The plasma display drive circuit diagram in the example 2 of this invention
[Drawing 4] The plasma display drive circuit diagram in the example 3 of this invention
[Drawing 5] The voltage-waveform view showing one example of the drive method of the plasma display panel in the example 3 of this invention
[Drawing 6] The plasma display drive circuit diagram in the example 4 of this invention
[Drawing 7] The voltage-waveform view showing one example of the drive method of the plasma display panel in the example 4 of this invention
[Drawing 8] The plasma display drive circuit diagram in the example 5 of this invention
[Drawing 9] The voltage-waveform view showing one example of the drive method of the plasma display panel in the example 5 of this invention
[Drawing 10] Drawing showing the example of a plasma display
[Drawing 11] Drawing showing the example of a TV apparatus
[Drawing 12] Drawing showing the example of a computer apparatus
[Drawing 13] Plasma display drive circuit diagram
[Description of Notations]
Y1-Yn402 Scanning electrode
X, 401 Maintenance electrode
11 X Driver
12 Y Driver
111, 122, 3101, 608, 610, 807 Capacitor for recovery
115, 112A, 112B, 114A, 114B, 123A, 123B, 125A, 125B, 341A-34nA, 341B-34nB, 3102, 3103, 3107, 3108, 3202, 3203, 404, 413, 414, 417, 418, 611, 612, 613, 810, 811, 812, 813, 814 Switching means
113, 124A, 124B, 3104, 405, 451, 809 Coil 121 Semiconductor integrated circuit
126A, 126B, 3109, 406, 455, 614, 816 Switch control means
31 Reactive Power Recovery Circuit
32 Output Circuit of Driver IC
3105 High Potential Side Power Supply
3106 3110 Low voltage side power supply
3111 Output of Reactive Power Recovery Circuit
3201 806 Input terminal
3204 High Potential Side Power Terminal
3205 Low Voltage Side Power Terminal
32 Output Circuit of Driver IC
33,815 Output terminal
34 Load-carrying Capacity
4101 Driver Circuit
410 Power Circuit Means
410A, 410B Power supply means
412, 413, 415, 416 Voltage generating means
411 Power Supply Generating Means
420 Leak Switching Means
450 Power Recovery Circuit
454 Capacitor
601 801 Quantity withstand voltage IC
602 802 Terminal which impresses the direct current voltage for charge recovery

603 803 Direct-current-voltage terminal
604 805 Earth terminal of IC
609 808 Auxiliary capacitor
615 Terminal Which Connects Drive Circuit with IC
616 Terminal of Data Electrode
804 Terminal for Charge Recovery of IC

[Translation done.]

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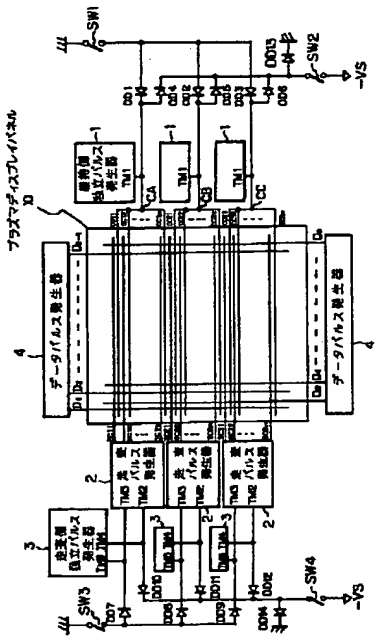
(54) DRIVING CIRCUIT FOR PLASMA DISPLAY PANEL

(57) Abstract:

PROBLEM TO BE SOLVED: To eliminate luminance variation between scanning electrode blocks or maintenance electrode blocks in the plasma display panel driving circuit which uses the scanning electrode blocks and maintenance electrode blocks.

SOLUTION: A switch SW1 is connected to the high-potential side for maintenance pulses and supplies a maintenance pulse current to a maintenance electrode, and a switch SW2 is connected to the low-potential side of the power source for maintenance pulses and draws the maintenance pulse current out of the maintenance electrode. A switch SW3 is connected to the high-potential side of the power source for maintenance pulses and supplies the maintenance pulse current to a scanning electrode and a switch SW4 is connected to the low potential side of the power source for maintenance pulses and draws the maintenance pulse current out of the scanning electrode. Diodes DD1 to DD6 are so provided that pulses which should be generated independently at the respective maintenance blocks does flow round to other maintenance electrode blocks. Further, diodes DD7 to DD12 are so provided that pulses which should be generated independently at the respective scanning electrode blocks of not flow to other scanning electrode blocks.



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(54)【発明の名称】　プラズマディスプレイパネルの駆動回路

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(57)【特許請求の範囲】

【請求項１】　縞状の走査電極と、前記走査電極に直交する縞状の列電極とを備えるプラズマディスプレイパネルの前記走査電極が複数のブロックに分割され、前記各走査電極ブロック毎に予備放電期間、書込期間を有し、全ての前記走査電極に共通の維持期間を少なくとも有するプラズマディスプレイパネルの駆動回路において、

維持期間においてプラズマディスプレイパネルに印加する維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の高電位側に接続され、プラズマディスプレイパネルに向かって電流を供給するプルアップスイッチの他端に、前記走査電極ブロックの数に等しい数のダイオードからなる第１のダイオード群のアノードが共通接続され、前記第１のダイオード群の個別のカソードが前記各走査電極ブロックに対応する走査パルス発

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生器に接続され、

維持期間においてプラズマディスプレイパネルに印加する維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の低電位側に接続され、プラズマディスプレイパネルより電流を吸い込むプルダウンスイッチの他端に、前記走査電極ブロックの数に等しい数のダイオードからなる第２のダイオード群のカソードが共通接続され、前記第２のダイオード群の個別のアノードが前記各走査電極ブロックに対応する走査パルス発生器に接続され、

前記維持パルス以外のパルスで、各走査電極ブロック毎に独立して必要なパルスを発生するスイッチが、各走査電極ブロック毎に設けられていることを特徴とする、プラズマディスプレイパネルの駆動回路。

【請求項２】　縞状の走査電極と、前記走査電極とペア

となり前記走査電極に並行する縞状の維持電極と、前記走査電極および前記維持電極に直交する縞状の列電極とを備えるプラズマディスプレイパネルの、前記走査電極および前記維持電極のペアが複数のブロックに分割され、このブロックに対応して走査電極ブロックと維持電極ブロックを有し、前記各ブロック毎に予備放電期間、書込期間を有し、全ての前記走査電極および前記維持電極に共通の維持期間を少なくとも有するプラズマディスプレイパネルの駆動回路において、

維持期間においてプラズマディスプレイパネルに印加する走査電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の高電位側に接続され、プラズマディスプレイパネルに向かって電流を供給するプルアップスイッチの他端に、前記走査電極ブロックの数に等しい数のダイオードからなる第１のダイオード群のアノードが共通接続され、前記第１のダイオード群の個別のカソードが各走査電極ブロックに対応する走査パルス発生器に接続され、

維持期間においてプラズマディスプレイパネルに印加する走査電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の低電位側に接続され、プラズマディスプレイパネルより電流を吸い込むプルダウンスイッチの他端に、前記走査電極ブロックの数に等しい数のダイオードからなる第２のダイオード群のカソードが共通接続され、前記第２のダイオード群の個別のアノードが、前記各走査電極ブロックに対応する走査パルス発生器に接続され、

維持期間においてプラズマディスプレイパネルに印加する維持電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の高電位側に接続され、プラズマディスプレイパネルに向かって電流を供給するプルアップスイッチの他端に、前記維持電極ブロックの数に等しい数のダイオードからなる第３のダイオード群のアノードが共通接続され、前記第３のダイオード群の個別のカソードが前記各維持電極ブロックに接続され、

維持期間においてプラズマディスプレイパネルに印加する維持電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の低電位側に接続され、プラズマディスプレイパネルより電流を吸い込むプルダウンスイッチの他端に、前記維持電極ブロックの数に等しい数のダイオードからなる第４のダイオード群のカソードが共通接続され、前記第４のダイオード群の個別のアノードが前記各維持電極ブロックに接続され、

前記維持パルス以外のパルスで、各走査電極ブロック毎に独立して必要なパルスを発生するスイッチが各走査電極ブロック毎に設けられ、

前記維持パルス以外のパルスで、各維持電極ブロック毎に独立して必要なパルスを発生するスイッチが各維持電極毎に設けられていることを特徴とする、プラズマディスプレイパネルの駆動回路。

【請求項３】　前記走査側維持パルス発生回路のプルアップスイッチと前記維持側維持パルス発生回路のプルダウンスイッチが第１の電荷回収回路により結合され、前記走査側維持パルス発生回路のプルダウンスイッチと前記維持側維持パルス発生回路のプルアップスイッチが第２の電荷回収回路により結合されている請求項２に記載のプラズマディスプレイパネルの駆動回路。

【請求項４】　第１、第２の電荷回収回路は維持パルスの立ち上がりでオンするスイッチと、コイルからなる、請求項３のプラズマディスプレイパネルの駆動回路。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明はプラズマディスプレイパネルに関し、特にＡＣメモリ型プラズマディスプレイパネルの駆動回路に関する。

【０００２】

【従来の技術】プラズマディスプレイパネルは構造が簡単で大面積化が容易であり、またパネルを作成する基板として窓ガラスなどに広範に用いられている安価なソーダガラスを用いることができるなどの利点を有している。

【０００３】プラズマディスプレイパネルはこのソーダガラスよりなる２枚の絶縁基板を用い、それぞれの絶縁基板上に、電極や表示の単位となる画素を区切るための隔壁などを形成し、これら構造物を形成した２枚の絶縁基板を張り合わせ、放電用のガスを封入して完成する。隔壁の高さは一般に０．２ｍｍ程度であり、絶縁基板の厚さは３ｍｍ程度であるから、非常に薄型で軽量のディスプレイを作ることができる。

【０００４】したがって、このような特徴を生かして、プラズマディスプレイパネルは特に近年進展が著しいパーソナルコンピュータやオフィスワークステーション、ないしは発展が期待されている大画面の壁掛けテレビなどに用いられようとしている。

【０００５】プラズマディスプレイは、大別してＤＣ型とＡＣ型に分類される。ＤＣ型は電極が直接放電ガスに接しており、一度放電が起こるとＤＣ電流が流れ続けるためＤＣ型と呼ばれる。一方、ＡＣ型は、電極と放電ガスの間に絶縁層が介在するので、電流は電圧印加後１マイクロ秒程度の短時間パルス状に流れて収束してしまう。絶縁層はコンデンサとして働くので、ＡＣパルスを印加することによりパルス状の発光が繰り返され、表示がなされる。このためＡＣ型と呼ばれる。

【０００６】ＤＣ型は構造が簡単であるが、電極が直接放電にさらされるため電極の消耗が激しく長寿命を得ることが難しい。ＡＣ型は絶縁層を形成する手間と費用がかかるが、電極が絶縁層で覆われているため寿命が長い。また、高輝度発光を可能にするメモリと呼ばれる機能を容易に実現できるため近年開発が進んでいる。本願

発明は、このＡＣメモリ型プラズマディスプレイパネルを用いている。

【０００７】そこで、以下でＡＣメモリ型プラズマディスプレイパネルの構造を説明し、さらにその駆動方法と従来の駆動回路について説明する。

【０００８】図８は特開平７－２９５５０６号公報に示されている一般的なＡＣメモリ型プラズマディスプレイパネルの構造を示したもので、本願発明および従来の駆動回路の適用対象とするものである。図８（ａ）は平面図、図８（ｂ）は図８（ａ）のＸ－Ｘ’線断面図である。

【０００９】このプラズマディスプレイパネルは、３ｍｍ厚のソーダガラスよりなる第１絶縁基板１１と、同じく３ｍｍ厚のソーダガラスよりなる第２絶縁基板１２と、透明なネサ膜よりなる縞状の維持電極１３ａと、同じく透明なネサ膜よりなる縞状の走査電極１３ｂと、透明な維持電極１３ａや透明な走査電極１３ｂに十分な電流を供給するための銀の厚膜よりなる金属電極１３ｃと、銀の厚膜よりなる縞状の列電極１４と、全圧で５００Ｔｏｒｒで3％のＸｅを混合した、７対３のＨｅとＮｅよりなる放電ガスが充填される放電ガス空間１５と、放電ガス空間を確保するとともに画素を区切る厚膜の隔壁１６と、放電ガスの放電により発生する紫外光を可視光に変換するZn_2SiO_4：Ｍｎなどよりなる蛍光体１７と、維持電極１３ａ、走査電極１３ｂ、および金属電極１３ｃを覆う厚膜の透明グレーズよりなる絶縁層１８ａと、列電極１４を覆う厚膜の絶縁層１８ｂ、および絶縁層１８ａを放電より保護する厚さ２μｍのＭｇＯよりなる保護層１９で構成される。なお、図８（ａ）において、縦・横の隔壁１６で囲まれた区画が画素２０となる。走査電極S_i（ｉ＝１，２，・・・，ｍ）と列電極D_j（ｊ＝１，２，・・・，ｎ）の交点の画素をa_{ij}で示す。図８（ｂ）の蛍光体１７を画素毎に赤、緑、青の３色に塗り分ければ、フルカラー表示可能なプラズマディスプレイパネルが得られる。このプラズマディスプレイパネルの表示方向は、図８（ｂ）の上面あるいは下面のどちらでも可能であるが、この例の場合は下面の方が開口率が高く、蛍光体の発光部分を直接目視するスタイルとなり、より高い輝度を得られので好ましい。

【００１０】次に、プラズマディスプレイパネルの電極のみに着目した平面図を図９に示す。図９において、１０はプラズマディスプレイパネル、２１は第１絶縁基板１１と第２絶縁基板１２を張り合わせ、内部に放電ガスを封入し気密にシールするシール部、C_1，C_2，・・・，C_mは維持電極１３ａ、S_1，S_2，・・・，S_mは走査電極１３ｂ、D_1，D_2，・・・，D_{n-1}，D_nは列電極１４である。

【００１１】実際のプラズマディスプレイパネルとしては、例えば走査電極S_1，S_2，・・・，S_mは４８０本、維持電極C_1，C_2，・・・，C_mは４８０本、列

電極D_1，D_2，・・・，D_{n-1}，D_nは１９２０本である。各画素のピッチは、列電極間は０．３５ｍｍ、走査電極間は１．０５ｍｍである。走査電極と列電極の距離は０．２ｍｍである。

【００１２】次に、このようなプラズマディスプレイパネルを用いて階調表示を行う方法を説明する。プラズマディスプレイパネルでは、他のデバイスと異なり印加電圧の変更により高輝度の階調表示を行うことは困難であり、一般的には発光回数を制御して階調表示を行う。特に、高輝度の階調表示を行うには以下で述べるサブフィールド法が用いられる。

【００１３】図１０において、横軸は時間であり、縦軸は走査電極を表している。１フィールドの間に１枚の画像が送られる。１フィールドの時間は個々のコンピュータや放送システムによって異なるが、大体１／５０秒から１／７５秒の範囲内に設定されていることが多い。

【００１４】プラズマディスプレイパネルによる階調画像表示では、図１０のように１フィールドをｋ個のサブフィールド（図１０の場合はＳＦ１～ＳＦ６のｋ＝６個のサブフィールド）に分割している。各サブフィールドは、図１１で説明する表示発光のための維持放電期間および維持放電以外の予備放電、予備放電消去、走査などの期間を含む書き込み放電制御期間より構成されている。各画素の発光輝度はそれぞれのサブフィールドＳＦ１～ＳＦ６における各画素の維持放電の発光回数を2^nで重みづけて、次のように制御する。

【００１５】

【数１】

$$\text{輝度}=\sum_{n=1}^{k}(L_1\times 2^{n-1})\times a_n$$

ｎはサブフィールドの番号であり、もっとも輝度が低いサブフィールドを１、もっとも輝度が高いサブフィールドをｋとする。L_1はもっとも輝度が低いサブフィールドの輝度であり、a_nは１または０の値をとる変数で、ｎ番目のサブフィールドにおいて当該画素を発光させる場合は１、発光させない場合はゼロである。各サブフィールドの発光輝度が異なることから、各サブフィールドの点灯／非点灯を選択することで、輝度を制御できる。

【００１６】図１０はｋ＝６の場合を示しているので、赤、緑、青のカラー画素を一組としてカラー表示を行う場合は、各色で$2^k=2^6=64$段階の階調表現ができる。色数としては、$64^3=262144$色（黒を含む）の表示ができる。ｋ＝１であれば、１フィールド＝１サブフィールドであり、各色で２階調（オンかオフ）の表示ができる。色数としては$2^3=8$色（黒を含む）の表示ができる。

【００１７】図１１は、図８、図９に示したプラズマディスプレイパネルの１つのサブフィールドにおける駆動電圧波形および発光波形の一例を示す図である。

【００１８】波形Ａは維持電極C_1，C_2，・・・，Ｃ

$_m$ に印加する電圧波形、波形Ｂは走査電極S_1に印加する電圧波形、波形Ｃは走査電極S_2に印加する電圧波形、波形Ｄは走査電極S_mに印加する電圧波形、波形Ｅは列電極D_1に印加する電圧波形、波形Ｆは列電極D_2に印加する電圧波形、波形Ｇは画素a_{11}の発光波形を示している。波形Ｅや波形Ｆの斜線を有するパルスは、書き込みすべきデータの有無にしたがってパルスの有無が決定されていることを示す。データ電圧波形として、図１１では画素a_{11}，a_{22}にデータを書き込む場合を示している。３行目以降の画素については、データの有無により表示が行われることを示している。

【００１９】維持電極C_1，C_2，・・・，C_mには維持パルス３１と予備放電パルス３６が印加される。また、走査電極S_1，S_2，・・・，S_mには、これらの電極に共通した維持パルス３２、消去パルス３５および予備放電消去パルス３７のほかに、各走査電極に独立したタイミングで走査パルス３３が線順次に印加される。各列電極Ｄｊ（ｊ＝１，２，・・・，ｎ）には、発光データがある場合は、データパルス３４が走査パルス３３に同期して印加される。

【００２０】図８、図９に示した構成のプラズマディスプレイパネルにおいては、まず消去パルス３５によって、直前のサブフィールドで発光していた画素を消去する。次に、予備放電パルス３６により、全ての画素を１度強制的に放電させ、さらに予備放電消去パルス３７で予備放電を消す。これにより、次に印加する走査パルスでの書き込み放電を起こり易くしている。

【００２１】予備放電を消去後、走査電極と列電極の間に同じタイミングで走査パルス３３とデータパルス３４を印加して書き込み放電を行わせると、その後は隣り合う維持電極と走査電極の間で、維持パルス３１と維持パルス３２により維持放電が持続される。また、走査パルス３３のみ、またはデータパルス３４のみが印加された場合は書き込み放電は発生せず、その後の維持放電も発生しない。このような機能はメモリ機能と呼ばれる。維持放電の回数により、各サブフィールドの発光輝度が制御される。

【００２２】次に、図１２に、プラズマディスプレイパネルの異なる駆動法の例を示す（特開平０４－４２２８９号公報）。T_1～T_6はサブフィールドを表わしている。図１２では、書き込み放電のタイミングとともに、維持放電の消去タイミングも走査されている。また、予備放電は１フィールドに１回としている。この図１２に対応する１つのサブフィールドの駆動波形を図１３に示す。図１１と異なり、維持パルスが継続的に印加されている。また、１つの維持パルス周期の中に３つの走査パルスが印加され、これと同期してデータパルスが印加される。データパルスは維持パルスや消去パルスと重ならないようにしている。消去パルスは、この３つの走査パルスに対応して、３つの走査電極に同時に印加され、これを一組として走査されている。

【００２３】最後に、このような駆動波形を生成する回路について説明する。図１１からわかるように維持パルス３１，３２はそれぞれ維持電極C_1，C_2，・・・，C_mと走査電極S_1，S_2，・・・，S_mに共通に印加される。したがって、維持パルスを発生する回路は全画面に共通でよい。例えば、大塚晃、「大画面ａｃ形カラープラズマディスプレイ　－現状と将来展望－」（サイエンス・コミュニケーションズ・インターナショナル株式会社発行の雑誌「ディスプレイ　アンド　イメージング（日本版）：１９９６年、第４巻、６７から７３頁）のＦｉｇ．３を参照すると、維持電極側の維持パルス３１を発生する回路は「Ｘ　ＳＵＳＴＡＩＮ　ＰＵＬＳＥＲ」と記され、全画面に一括して印加されている。また、走査電極側の維持パルス３２を発生する回路は「Ｙ　ＳＵＳＴＡＩＮ　ＰＵＬＳＥＲ」と記され、やはり全画面に一括印加されている。

【００２４】ところで、書き込み放電を確実に起こすには予備放電消去パルス３７を印加してから、走査パルス３３を印加するまでの時間をできるだけ短くした方がよいことが知られている。また、書き込み放電後、維持放電を確実に起こすには書き込み放電から維持放電までの時間をできるだけ短くした方がよいことが知られている（特開平７－１９１６２７号公報）。

【００２５】図１４は特開平７－１９１６２７号公報の図１に記されている第１の技術例の駆動方法を示す図で、１つのサブフィールドの駆動状態を示しており、Ａ１は予備放電パルスを印加する期間、Ｂ１は予備放電消去パルスを印加する期間、Ｃ１１，Ｃ１２，Ｃ１３は書き込み放電期間、Ｅ１１，Ｅ１２，Ｅ１３は第１維持放電期間、Ｄ１は第２維持放電期間を示す。

【００２６】走査電極S_1，S_2，・・・，S_mは３つの走査電極ブロックＧ，Ｈ，Ｉに分けられている。また、図示されていないが、走査電極S_1～S_mとペアで配列されている維持電極C_1～C_mも、走査電極ブロックＧ，Ｈ，Ｉに対応して３つの維持電極ブロックにまとめられている。

【００２７】図１４では、書き込み放電から維持放電までの期間を短くするために、各走査電極ブロックでの書き込み動作が終了した直後に各走査電極ブロック毎、または各維持電極ブロック毎に独立の第１維持放電期間Ｅ１１，Ｅ１２，Ｅ１３を設けている。

【００２８】次に、図１４に対応する駆動波形の例（特開平７－１９１６２７号公報の図３）を図１５に示す。図１５において、Ａ７が予備放電パルスを印加する期間、Ｂ７は予備放電消去パルスを印加する期間、Ｃ７１，Ｃ７２，Ｃ７３は書き込み放電期間、Ｅ７１，Ｅ７２，Ｅ７３は第１維持放電期間、Ｄ７が第２維持放電期間を示す。

【００２９】また、ＣＯＭ１，ＣＯＭ２，ＣＯＭ３は各

維持電極ブロックに印加する維持電極駆動波形、Ｓ１１，Ｓ１２は走査電極ブロックＧの最初の走査電極と次の走査電極に印加する駆動電圧波形、Ｓ２１，Ｓ２２は走査電極ブロックＨの最初の走査電極と次の走査電極に印加する駆動電圧波形、Ｓ３１，Ｓ３２は走査電極ブロックＩの最初の走査電極と次の走査電極に印加する駆動電圧波形、ＤＡＴＡは、データ電極に印加する駆動電圧波形を示す。

【００３０】図１５から明らかなように第１の維持放電期間Ｅ７１，Ｅ７２，Ｅ７３は各走査電極ブロック毎および各維持電極ブロック毎に独立しているので、各維持電極ブロックの維持電極駆動波形ＣＯＭ１，ＣＯＭ２，ＣＯＭ３に示される維持パルス４１は各維持電極ブロック毎に独立している。同様に、各走査電極ブロックの走査電極駆動波形Ｓ１１，Ｓ１２，Ｓ２１，Ｓ２２，Ｓ３１，Ｓ３２に示される維持パルス４２は各走査電極ブロック毎に独立している。

【００３１】このように、書き込み放電を確実に起こし、また書き込み放電から維持放電への移行を確実にするには、走査電極ブロックと維持電極ブロックを用いた駆動法を用いるとよい。この場合、各走査電極ブロックおよび維持電極ブロックにおいて用いる維持パルスが独立に制御される必要があるので、各走査電極ブロック、各維持電極ブロックに対応する維持電極側、走査電極側それぞれの維持パルスの発生回路はそれぞれの走査電極ブロックおよび維持電極ブロック毎に独立して設けていた。この場合の回路構成図を図１６に示す。

【００３２】図１６の回路は、走査パルス３３を発生する走査パルス発生器２と、データパルスを発生するデータパルス発生器４、予備放電消去パルス３７や、各維持電極ブロックに独立の維持パルス４１、および維持パルス３１を発生する維持側共通パルス発生器３９と、予備放電パルス３６を発生するとともに、各走査電極ブロックに独立の維持パルス４２および維持パルス３２を発生する走査側共通パルス発生器４０で構成されている。維持電極１３ａは走査電極ブロックに対応する３つの維持電極ブロックＣＣ１１～ＣＣ１ｍ，ＣＣ２１～ＣＣ２ｍに分けられ、それぞれのブロックで共通に電極ＣＡ，ＣＢ，ＣＣに接続されている。

【００３３】

【発明が解決しようとする課題】上記引用した特開平７－１９１６２７号公報に示されているように、書き込み放電を確実に起こし、あるいは書き込み放電から維持放電への移行を確実にして書き込みミスをなくするには、走査電極ブロックと維持電極ブロックを用いた駆動法を用いるとよい。

【００３４】ただし、この場合、各走査電極ブロックおよび各維持電極ブロックにおいて用いる維持パルスが独立に制御される必要があるので、各走査電極ブロック、および各維持電極ブロックそれぞれの維持パルスの発生

回路はそれぞれの走査電極ブロック、維持電極ブロック毎に独立して設けられていた。

【００３５】しかしながら、このように走査電極ブロックおよび維持電極ブロックを用いた駆動方法を実際に実現するために、各走査電極ブロックおよび維持電極ブロックの維持電極側、走査電極側それぞれに独立した維持パルス発生回路を備えてプラズマディスプレイパネルを駆動すると、維持パルス発生回路はそれぞれの走査電極ブロックおよび維持電極ブロック毎に独立して設けられているので、各走査電極ブロック、維持電極ブロック毎の発光する画素数が異なると、各走査電極ブロックおよび各維持電極ブロック毎に輝度が変化するという問題が発生した。以下で、このような走査電極ブロック、または維持電極ブロック毎の輝度差が発生する原因を説明する。

【００３６】図１７は、図１５に示す駆動波形を発生する図１６の回路図において、維持側共通パルス発生器３９、または走査側共通パルス発生器４０に使用される走査側、または維持側の維持パルス発生回路の基本回路図である。この回路はプルアップスイッチとして働くＰチャンネルＦＥＴ５１と、プルダウンスイチッチとして働くＮチャンネルＦＥＴ５２と、電解コンデンサ５３と、セラミックやフィルムなどの小容量のコンデンサ５４とで構成される。なお、ＰＰ１，ＰＰ２は電圧測定ポイント、－ＶＳ電源は維持電圧－ＶＳを与える電源端子である。

【００３７】図１７において、電解コンデンサ５３は１０μＦ以上の静電容量をもつ。プラズマディスプレイパネルの静電容量は１０ｎＦ程度であるから、電解コンデンサ５３の静電容量はプラズマディスプレイパネルの静電容量の１０００倍以上であり、その上に１００ＫＨｚ以上の高周波成分は小容量コンデンサ５４によってバイパスされる。したがって、プラズマディスプレイパネルに発光電流を供給する場合でも、ポイントＰＰ１の電位変動は小さい。

【００３８】これに対して、ＮチャンネルＦＥＴ５２のオン抵抗はピーク電流２０Ａ程度に対して０．５オーム程度であり、１０Ｖほどの電圧降下を生じる。経済性を無視すればさらに大電流容量でオン抵抗が小さいＦＥＴなどのスイッチ素子を用いることは可能だが、経済的な価格、および適当な大きさのＦＥＴということになるとこの程度のオン抵抗のＦＥＴで妥協する必要がある。

【００３９】以上のように、放電発光が起こった場合に維持パルスを発生させる部分の電圧降下は主としてＦＥＴなどのスイッチで生じる。

【００４０】図１８は、図１７の回路を用いた場合において、発光する画素数が少ない走査電極ブロックおよび維持電極ブロックの維持パルス発生回路の電圧波形（同図（ａ））、発光する画素数が多い走査電極ブロックおよび維持電極ブロックの維持パルス発生回路の電圧波形

であり（同図（ｂ））、６０は維持パルス、６１－６４は放電発光のタイミングにおける電圧の窪みを示す。

【００４１】図１８に示したように、発光する画素数が少ない（図１８（ａ））場合は、ＮチャンネルＦＥＴ５２での電圧降下は少なく、ポイントＰＰ２における放電発光での電圧降下により生ずる電圧の窪み６２は小さい。一方、発光する画素数の多い（図１８（ｂ））場合は、ポイントＰＰ１の電位変動は相変わらず小さいが、ＮチャンネルＦＥＴ５２における電圧降下が大きく、ポイントＰＰ２における放電発光での電圧降下により生ずる電圧の窪み６４は１０Ｖ以上と大きくなる。

【００４２】このため、発光する画素数の少ない走査電極ブロックまたは維持電極ブロックでは電圧の窪み６２が小さく発光する画素に十分な電圧が印加されるために発光輝度が高くなるが、発光する画素数の多い走査電極ブロックおよび維持電極ブロックでは電圧の窪み６４が大きく発光する画素に十分な電圧が印加されないために発光輝度が低くなる。

【００４３】このような現象を低減するには、維持パルスを発生する回路の内部抵抗を十分小さくすればよい。具体的には、維持パルスを発生する回路内で多くの電圧降下が生ずるパワーＭＯＳＦＥＴなどのスイッチ素子の内部抵抗を十分小さくすればよい。しかしながら、このようにすると前記スイッチ素子の大きさを極端に大きくしなければならず、維持パルス発生回路の大きさが極端に大きくなるだけでなく、スイッチ素子やスイッチ素子を駆動するための駆動回路の価格が極端に高くなり、実用に供することができなくなる。

【００４４】したがって、物理的な大きさや、経済性の観点からみた場合、従来用いることができる技術範囲内では、各走査電極ブロックおよび維持電極ブロック毎に発光する画素数が大きく異なる場合、各走査電極ブロックまたは維持電極ブロック毎の輝度が異なってしまう問題を生じていた。

【００４５】各走査電極ブロックまたは維持電極ブロック毎の輝度が異なると、走査電極ブロックまたは維持電極ブロック間に明瞭に輝度差が認められる。これは特に表示技術に深く関係している人だけでなく、一般にディスプレイを用いる人であれば直ちに認識できる。この走査電極ブロックまたは維持電極ブロック毎の輝度差は、元の画像には含まれないものであり、表示される画像は偽物の画像となってしまう。自然画の表示では特に目立つものであり、自然画の表示品位を完全に損なうものである。これはディスプレイとしては致命的な欠点であり、ディスプレイの商品としての価値をゼロにしてしまう重大な欠点である。

【００４６】本発明の目的は、書き込み放電や、書き込み放電から維持放電への移行を確実にでき、その結果プラズマディスプレイパネルの書き込みミスをなくすことができる、走査電極ブロックと、維持電極ブロックを用

いた駆動方法を用いる場合に、従来並の回路の大きさと価格を維持しつつ、走査電極ブロック、または維持電極ブロック毎の輝度変動を解消できる、プラズマディスプレイパネルの駆動回路を提供することにある。

【００４７】

【課題を解決するための手段】本発明のプラズマディスプレイパネルの駆動回路は、縞状の走査電極と、走査電極に直交する縞状の列電極とを備えるプラズマディスプレイパネルの前記走査電極が複数のブロックに分割され、前記各走査電極ブロック毎に予備放電期間、書込期間を有し、全ての前記走査電極に共通の維持期間を少なくとも有するプラズマディスプレイパネルの駆動回路において、維持期間においてプラズマディスプレイパネルに印加する維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の高電位側に接続され、プラズマディスプレイパネルに向かって電流を供給するプルアップスイッチの他端に、前記走査電極ブロックの数に等しい数のダイオードからなる第１のダイオード群のアノードが共通接続され、前記第１のダイオード群の個別のカソードが前記各走査電極ブロックに対応する走査パルス発生器に接続され、維持期間においてプラズマディスプレイパネルに印加する維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の低電位側に接続され、プラズマディスプレイパネルより電流を吸い込むプルダウンスイッチの他端に、前記走査電極ブロックの数に等しい数のダイオードからなる第２のダイオード群のカソードが共通接続され、前記第２のダイオード群の個別のアノードが前記各走査電極ブロックに対応する走査パルス発生器に接続され、上記の維持パルス以外のパルスで、各走査電極ブロック毎に独立して必要なパルスを発生するスイッチが、各走査電極ブロック毎に設けられている。

【００４８】本駆動回路は維持電極無し（対向放電型）の場合を示している。

【００４９】また、本発明の他のプラズマディスプレイパネルの駆動回路は、縞状の走査電極と、前記走査電極とペアとなり前記走査電極に並行する縞状の維持電極と、前記走査電極および前記維持電極に直交する縞状の列電極とを備えるプラズマディスプレイパネルの、前記走査電極および前記維持電極のペアが複数のブロックに分割され、このブロックに対応して走査電極ブロックと維持電極ブロックを有し、前記各ブロック毎に予備放電期間、書込期間を有し、全ての前記走査電極および前記維持電極に共通の維持期間を少なくとも有するプラズマディスプレイパネルの駆動回路において、維持期間においてプラズマディスプレイパネルに印加する走査電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の高電位側に接続され、プラズマディスプレイパネルに向かって電流を供給するプルアップスイッチの他端に、前記走査電極ブロックの数に等しい

数のダイオードからなる第１のダイオード群のアノードが共通接続され、前記第１のダイオード群の個別のカソードが各走査電極ブロックに対応する走査パルス発生器に接続され、維持期間においてプラズマディスプレイパネルに印加する走査電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の低電位側に接続され、プラズマディスプレイパネルより電流を吸い込むプルダウンスイッチの他端に、前記走査電極ブロックの数に等しい数のダイオードからなる第２のダイオード群のカソードが共通接続され、前記第２のダイオード群の個別のアノードが、前記各走査電極ブロックに対応する走査パルス発生器に接続され、維持期間においてプラズマディスプレイパネルに印加する維持電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の高電位側に接続され、プラズマディスプレイパネルに向かって電流を供給するプルアップスイッチの他端に、前記維持電極ブロックの数に等しい数のダイオードからなる第３のダイオード群のアノードが共通接続され、前記第３のダイオード群の個別のカソードが前記各維持電極ブロックに接続され、維持期間においてプラズマディスプレイパネルに印加する維持電極側の維持パルスを発生するためのスイッチであって、一端が維持パルス用電源の低電位側に接続され、プラズマディスプレイパネルより電流を吸い込むプルダウンスイッチの他端に、前記維持電極ブロックの数に等しい数のダイオードからなる第４のダイオード群のカソードが共通接続され、前記第４のダイオード群の個別のアノードが前記各維持電極ブロックに接続され、上記の維持パルス以外のパルスで、各走査電極ブロック毎に独立して必要なパルスを発生するスイッチが各走査電極ブロック毎に設けられ、上記の維持パルス以外のパルスで、各維持電極ブロック毎に独立して必要なパルスを発生するスイッチが各維持電極毎に設けられている。

【００５０】また、本発明の実施態様によれば、前記走査側維持パルス発生回路のプルアップスイッチと前記維持側維持パルス発生回路のプルダウンスイッチが第１の電荷回収回路により結合され、前記走査側維持パルス発生回路のプルダウンスイッチと前記維持側維持パルス発生回路のプルアップスイッチが第２の電荷回収回路により結合されている。

【００５１】上述の回路構成をとることにより、従来技術の問題である走査電極ブロックまたは維持電極ブロック間の輝度差を完全に解消することができる。すなわち、従来は走査電極ブロックおよび維持電極ブロック毎に独立して設けられていた維持パルス発生のためのスイッチをプラズマディスプレイパネル全面で共通化したことにより、たとえ維持パルスを発生するスイッチの抵抗が少々大きくとも、どのブロックに印加される維持パルス電圧波形も同じものとなる。したがって、維持パルスを発生するスイッチとして、特別に低抵抗で高価な部品

を用いずとも、各ブロック間の輝度むらを解消できる。

【００５２】本発明のこの方法は、原理的に各ブロックに印加される維持パルス電圧波形を等しくするものであるから、その効果が完全であることも大きな特徴である。

【００５３】ただし、維持パルス共通化のために単純に各ブロック間を電気的に接続してしまっては、各走査電極ブロックまたは維持電極ブロック毎に独立に印加すべきパルスを生成できなくなるので、共通化された維持パルス発生スイッチの出力をプルアップ用、プルダウン用に独立に分け、これらの出力をダイオードを利用して各走査電極ブロックまたは維持電極ブロックに供給するようにした。

【００５４】このように、非常に簡単なダイオードを用いた回路構成によりパネル全面に共通した維持パルスを供給できるようにしたことで、書き込み放電や、書き込み放電から維持放電への移行を確実にでき、その結果プラズマディスプレイパネルの書き込みミスをなくすことができる、走査電極ブロックと維持電極ブロックを用いた駆動方法を用いる場合に、従来、走査電極ブロックと維持電極ブロック毎に発生していた輝度差を完全に解消することができる。しかも、このための追加部品は各走査電極ブロックまたは維持電極ブロック１つについて２個の安価なダイオードのみでよいため、ほとんどコストアップないしで大きな効果が得られる。

【００５５】

【発明の実施の形態】次に、本発明の実施形態について図面を参照して説明する。

【００５６】図１は本発明の第１の実施形態のプラズマディスプレイパネルの駆動回路の基本回路図である。図１のプラズマディスプレイパネルの駆動回路は、予備放電パルス３６や、各維持電極ブロックに独立の維持パルス４１を発生する維持側独立パルス発生器１と、走査パルス３３を発生する走査パルス発生器２と、予備放電消去パルス３７を発生するとともに、書き込み放電期間中に直流の走査電圧を走査パルス発生器に供給する走査側独立パルス発生器３と、データパルス発生器４と、ダイオードＤＤ１～ＤＤ１４と、全面に共通の維持パルスを発生するためのスイッチＳＷ１～ＳＷ４で構成されている。

【００５７】スイッチＳＷ１は維持パルス用電源の高電位側（図１では接地側）に接続され、維持電極側に維持パルス電流を供給するプルアップスイッチである。スイッチＳＷ２は維持パルス用電源の低電位側（図１では－ＶＳで示される電源端子）に接続され、維持電極側から維持パルス電流を引き抜くプルダウンスイッチである。スイッチＳＷ３は維持パルス用電源の高電位側（図１では接地側）に接続され、走査電極側に維持パルス電流を供給するプルアップスイッチである。スイッチＳＷ４は維持パルス用電源の低電位側（図１では－ＶＳで示され

る電源端子）に接続され、走査電極側から維持パルス電流を引き抜くプルダウンスイッチである。

【００５８】維持電極は走査電極ブロックに対応してＣＣ１１，・・・，ＣＣ１ｍ，ＣＣ２１，・・・，ＣＣ２ｍ，ＣＣ３１，・・・，ＣＣ３ｍの３つの群に分けられ、それぞれの群で共通に電極ＣＡ，ＣＢ，ＣＣに接続されている。

【００５９】図１からわかるように、従来は各走査電極ブロックおよび維持電極ブロック毎に設置されていた維持パルス発生スイッチが、本実施形態では走査側、維持側ではそれぞれ共通化されている。ただし各維持電極ブロックで独立に発生すべきパルスが他の維持電極ブロックに回り込まないようにダイオードＤＤ１～ＤＤ６が設けられている。また、各走査電極ブロックで独立に発生すべきパルスが他の走査電極ブロックに回り込まないようにダイオードＤＤ７～ＤＤ１２が設けられている。

【００６０】このように非常に簡単な、ダイオードを用いた回路構成により、プラズマディスプレイパネル１０全面に共通した維持パルスを供給できるようになり、従来発生していた走査電極ブロックまたは維持電極ブロック毎の輝度むらを完全に解消することができた。

【００６１】図２（ａ）、図２（ｂ）、図２（ｃ）は、図１に示した基本回路図内の維持側独立パルス発生器１、走査パルス発生器２、走査側独立パルス発生器３のそれぞれの回路図である。維持側独立パルス発生器１は、端子ＴＭ１と、維持電圧を与える電源端子－ＶＳ間に設けられたスイッチＳＷ５、端子ＴＭ１と、予備放電電圧を与える電源端子－ＶＰ間に設けられたＳＷ６で構成されている。走査側独立パルス発生器３は、端子ＴＭ４と、予備放電消去電圧を与える電源端子－ＶＰＥ間に設けられたスイッチＳＷ７，接地と端子ＴＭ間に設けられたスイッチＳＷ８、端子ＴＭ５と、走査電極を与える電源端子－ＶＷ間に設けられたスイッチＳＷ９で構成されている。

【００６２】図３は本実施形態の駆動回路により発生する駆動シーケンスを示す。この図は１サブフィールド内の駆動シーケンスを示しており、特開平７－１９１６２７号公報の図７と同一である。走査電極は図１４と同様３つの走査電極ブロックＧ，Ｈ，Ｉおよび維持電極ブロックに分けられている。

【００６３】図３において、Ａ５１，Ａ５２，Ａ５３は各走査電極ブロックおよび維持電極ブロックに独立の予備放電パルスを印加する期間、Ｂ５１，Ｂ５２，Ｂ５３は各走査電極ブロックおよび維持電極ブロックに独立の予備放電消去パルスを印加する期間、Ｃ５１，Ｃ５２，Ｃ５３は書き込み放電期間、Ｅ５１，Ｅ５２，Ｅ５３は各走査電極ブロックおよび維持電極ブロックに独立の第１の維持放電期間、Ｄ５は第２維持放電期間を示す。また、走査電極S_1，S_2，・・・，S_mは３つの走査電極ブロックＧ，Ｈ，Ｉに分けられている。

【００６４】予備放電消去から書き込み放電までの時間を短くするために、各走査電極ブロックおよび維持電極ブロックに独立の予備放電、予備放電消去期間が設けられ、また、書き込み放電から維持放電までの期間を短くするために、各走査電極ブロックおよび維持電極ブロックでの書き込み動作が終了した直後に各走査電極ブロックおよび維持電極ブロック毎に独立の第１維持放電期間Ｅ５１，Ｅ５２，Ｅ５３が設けられている。

【００６５】図４は本実施形態の駆動回路により発生する駆動波形と、各スイッチの動作を示す。なお、この波形図は特開平７－１９１６２７号公報の図７の駆動シーケンスに対応するものであるが、特開平７－１９１６２７号公報には記載がないためここに記す。

【００６６】維持パルス３１はパルス幅２μ秒、周期６μ秒、電圧－１６０Ｖ、維持パルス３２のパルス幅、周期、電圧は維持パルス３１に同じ、走査パルス３３はパルス幅３μ秒、電圧－１８０Ｖ、データパルス３４は走査パルス３３と同じパルス幅で、電圧は＋７０Ｖ、予備放電パルス３６はパルス幅１０μ秒、電圧－３００Ｖ、予備放電消去パルス３７はパルス幅１μ秒、電圧－９０Ｖ、維持パルス４１はパルス幅２０μ秒、電圧－１６０Ｖとした。消去パルス３５はここで用いなかったが、用いてもよいことは言うまでもない。

【００６７】電極ＣＡ，ＣＢ，ＣＣには予備放電パルス３６、維持パルス４１、維持パルス３１を印加する。維持パルス３１は、この図４だけからは明らかではないが、上述したように全面に共通に印加する。

【００６８】また、走査電極ＳＣ１１，ＳＣ１２，・・・，ＳＣ１ｍ，ＳＣ２１，ＳＣ２２，・・・，ＳＣ２ｍ，ＳＣ３１，ＳＣ３２，・・・，ＳＣ３ｍにはこれらの電極に共通した維持パルス３２のほかに、各走査電極ブロックおよび維持電極ブロックにおいて独立したタイミングで予備放電消去パルス３７を、また各走査電極に独立したタイミングで走査パルス３３を線順次に印加している。データパルス３４は走査パルス３３と同期して印加している。

【００６９】次に、図４の下部に示した波形を用いて、維持パルスを発生するスイッチＳＷ１～ＳＷ４の動作を説明する。図３に示すシーケンス、図４に示す駆動波形を実現し、さらに維持パルス３１，３２を全面共通に印加できる駆動回路の基本構成を示す図１を参照すると、スイッチＳＷ１は予備放電パルス３６、維持パルス４１、維持パルス３１を出している期間以外はオン状態となり、電極ＣＡ，ＣＢ，ＣＣを接地電位に固定する。スイッチＳＷ２は維持パルス３１を発生する期間にオンとなり、電極ＣＡ，ＣＢ，ＣＣの共通の維持パルス電位とする。スイッチＳＷ３は、予備放電消去パルス３７、走査パルス３３、維持パルス３２を発生している期間以外はオン状態となり、走査電極ＳＣ１１，ＳＣ１２，・・・，ＳＣ１ｍ，Ｓ２１，Ｓ２２，・・・，Ｓ２ｍ，Ｓ３

１，Ｓ３２，・・・，Ｓ３ｍを接地電位に固定する。スイッチＳＷ４は維持パルス３２を発生する期間にオンとなり、前記走査電極を共通の維持パルス電位とする。

【００７０】以上、本実施形態によれば、ダイオードを利用して発光表示のための維持パルスのみをプラズマディスプレイパネルの全面に共通して印加するようにしたことで、書き込み動作を確実化するために採用した走査電極ブロックおよび維持電極ブロックの導入により必ず発生していた走査電極ブロックと維持電極ブロック間の輝度差を、わずかなコストで完全になくすことができるようになった。

【００７１】この効果は、従来スイッチとして使用しているＦＥＴの低抵抗化で走査電極ブロックおよび維持電極ブロック間の輝度むらを押える場合のコストアップに比較すると、非常に大きな改良である。また、たとえ低抵抗のＦＥＴを採用した場合でも、各走査電極ブロックおよび維持電極ブロック間の輝度むらを完全に押さえることは原理的に不可能であるが、本実施形態では維持パルスの発生スイッチが全面で共通化されているのでで原理的に輝度差が生ずることがなく表示品位の向上に大きく資するものである。

【００７２】図５は、電荷回収回路を含む、本発明の第２の実施形態のプラズマディスプレイパネルの駆動回路の回路図である。本実施形態では、特願平７－４１５３６号に記載の電荷回収回路を応用して、パネルの静電容量を充放電するエネルギーを回収し、消費電力を有効に削減している。

【００７３】図５においては、ダイオードＤＤ１０～ＤＤ１２のカソードにスイッチＳＷ１０が接続され、、その他端に電荷回収用のコイルＬ１が接続され、その他端がダイオードＤＤ１～ＤＤ３のアノードに接続されている。また、ダイオードＤＤ７～ＤＤ９のアノードにスイッチＳＷ１１が接続され、その他端に電荷回収用のコイルＬ２が接続され、その他端がダイオードＤＤ４～ＤＤ６のカソードに接続されている。その他の部分は図１と同じであるので説明は略する。

【００７４】次に、この回路の駆動波形と各スイッチの動作を図６により説明する。図６では、動作波形は図４と同じであるが、新たに追加したスイッチＳＷ１０とＳＷ１１の動作が追加してある。図６からわかるように、維持パルス３２の１番目が立ち上がる時点でスイッチＳＷ１１がオンとなる。以下同様に維持パルス３２の立ち上がり時点でスイッチＳＷ１１がオンとなる。ただし、維持パルス３２の最後では、維持パルスを停止するのでスイッチＳＷ１０はオフのままである。

【００７５】一方、維持パルス３１の１番目の立ち上がる時点でスイッチＳＷ１０がオンとなる。以下同様に維持パルス３１の立ち上がり時点でスイッチＳＷ１０がオンとなる。維持パルス３１の最後では、維持パルスはまだ停止せず、維持パルス３２の最後につながる。したがって、維持パルス３１の最後の立ち上がりではスイッチＳＷ１０はやはりオンとなる。

【００７６】最後に、図７により、スイッチＳＷ１～スイッチＳＷ４およびスイッチＳＷ１０、スイッチＳＷ１１の動作の関係を詳しく説明する。図７は図６の期間Ｄ５で維持パルスを連続的に発生している部分を拡大したものである。また、説明のため、コイルＬ１，Ｌ２を流れる電流波形が追加してある。電流の極性は図５の矢印方向を正としている。

【００７７】図７に示す範囲内では、時刻ｔ１以前では維持電極１３ａの電位はゼロであり、走査電極１３ｂの電位は負の維持パルス電位である。

【００７８】時刻ｔ１でスイッチＳＷ１，ＳＷ４はオフとなり、スイッチＳＷ１１のみがオンとなる。すると、維持電極１３ａからダイオードＤＤ４～ＤＤ６、コイルＬ２、スイッチＳＷ１１、ダイオードＤＤ７～ＤＤ９、走査パルス発生器２の端子ＴＭ３を通して走査電極１３ｂへと電流が流れ、維持電極１３ａ、走査電極１３ｂは逆極性に充電される。この電流はコイルＬ２とプラズマディスプレイパネルの静電容量が共振して流れている。

【００７９】その結果、維持電極１３ａの電位は下がり、逆に走査電極１３ｂの電位は上昇する。コイルＬ２を流れる共振電流が停止する時刻ｔ２においてスイッチ１１をオフするとともに、スイッチＳＷ２，ＳＷ３をオンとして、維持電極１３ａは負の維持パルス電位に、走査電極１３ｂはゼロ電位に固定される。

【００８０】時刻ｔ３までくると、スイッチＳＷ２，ＳＷ３はオフとなり、スイッチＳＷ１０のみがオンとなる。すると、走査電極１３ｂから走査パルス発生器２の端子ＴＭ２、ダイオードＤＤ１０～ＤＤ１２、スイッチＳＷ１０、コイルＬ１、ダイオードＤＤ１～ＤＤ３を通して維持電極１３ａへと共振電流が流れ、維持電極１３ａ、走査電極１３ｂは逆極性に充電される。

【００８１】その結果、維持電極１３ａの電位は上がり、逆に走査電極１３ｂの電位は下降する。コイルＬ１を流れる共振電流が停止する時刻ｔ４においてスイッチ１０をオフするとともに、スイッチＳＷ１、ＳＷ４をオンとして、維持電極１３ａはゼロ電位に、走査電極１３ｂは維持パルス電位に固定される。

【００８２】時刻ｔ５以降は時刻ｔ１以降の動作を繰り返す。

【００８３】以上のように、電荷回収回路を追加することにより、パネルの静電容量を充放電するエネルギーを有効に回収し、電力を節約してディスプレイを動作させることが可能となる。

【００８４】上記の説明ではスイッチＳＷ１１は共振電流がゼロになるタイミングｔ２でオフさせると説明したが、実際はｔ２以降さらにコイルＬ２を流れ続けようとする共振電流はダイオードＤＤ４～ＤＤ６、またはダイオードＤＤ７～ＤＤ９により阻止されるので、スイッチ

ＳＷ１１をオフするタイミングは時刻ｔ２～ｔ３の間であればよい。全く同様に、スイッチＳＷ１０をオフするタイミングは、時刻ｔ４～ｔ５の間であればよい。

【００８５】なお、上記実施形態で述べた回路で用いるスイッチ素子としては、高速で大電流をオン／オフできる電解効果トランジスタ（ＦＥＴ）があるが、必ずしもこれに限らず適当な動作スピードと電流供給能力をもつ素子であれば、バイポーラトランジスタ、サイリスタ、ＩＧＢＴなどを用いてもよいことは言うまでもない。また、本発明は維持電極がない場合（対向放電型）にも適用できる。

【００８６】

【発明の効果】以上説明したように、本発明は、従来は各走査電極ブロックおよび維持電極ブロック毎に設置されていた維持パルス発生スイッチを、プラズマディスプレイパネルの全面にわたって共通化し、各走査電極ブロックおよび維持電極ブロックで独立に発生すべきパルスについては、安価なダイオードを利用して他の走査電極ブロックおよび維持電極ブロックに回り込まないようにしたので、書き込み放電や、書き込み放電から維持放電への移行を確実にでき、その結果プラズマディスプレイパネルの書き込みをなくすことができる、走査電極ブロックおよび維持電極ブロックを用いた駆動方法を用いる場合に、従来走査電極ブロックおよび維持電極ブロック間に必ず発生していた輝度差を、非常にわずかなコストアップで完全になくすことができるようになり、走査電極ブロックと維持電極ブロックを用いた駆動法の表示品位を大きく改善でき、プラズマディスプレイパネルの実用化という点で大変大きな効果を有する。

【図面の簡単な説明】

【図１】本発明の第１の実施形態のプラズマディスプレイパネル駆動回路の基本回路図である。

【図２】図１の各ブロックの内容を示す図である。

【図３】図１の駆動回路を適用する駆動シーケンスを示す図である。

【図４】図１の駆動回路の駆動波形と各スイッチの動作を説明する図である。

【図５】本発明の第２の実施形態のプラズマディスプレイパネル駆動回路の回路図である。

【図６】第２の実施形態の駆動波形の各スイッチの動作を説明する図である。

【図７】図６の一部を拡大した駆動波形と各スイッチの動作説明図である。

【図８】従来および本発明に係わるプラズマディスプレイパネルの構造を示す平面図と断面図である。

【図９】電極配置に注目した図８に示したプラズマディスプレイパネルの回路構成を示す概念図である。

【図１０】走査と維持を分離したサブフィールド方式の説明図である。

【図１１】図１０の詳細な駆動電圧波形と発光波形を示す図である。

【図１２】走査と維持が混合されたサブフィールドの説明図である。

【図１３】図１２の詳細な駆動電圧波形図である。

【図１４】走査電極と維持電極を複数の走査電極ブロック、維持電極ブロックに分割し、書き込み放電から維持放電までの時間を短縮した場合の一つのサブフィールドの構成図である。

【図１５】図１４の駆動波形図である。

【図１６】図１５の駆動波形を発生する回路構成図である。

【図１７】走査電極ブロックまたは維持電極ブロックの維持パルス発生回路の基本回路図である。

【図１８】図１８（ａ）は、発光する画素数が少ない走査電極ブロックまたは維持電極ブロックの維持パルス発生回路の詳細な出力電圧波形図、図１８（ｂ）は発光する画素数が多い走査電極ブロックまたは維持電力ブロックの維持パルス発生回路の詳細な出力電圧波形図である。

【符号の説明】

１　維持側独立パルス発生器
２　走査パルス発生器
３　走査側独立パルス発生器
４　データパルス発生器
１０　プラズマディスプレイパネル
１１　第１絶縁基板
１２　第２絶縁基板
１３ａ，C_1，C_2，・・・，C_m　維持電極
１３ｂ，S_1，S_2，・・・，S_m　走査電極
１３ｃ　金属電極
１４，D_1，D_2，・・・，D_{n-1}，D_n　列電極
１５　放電ガス空間
１６　隔壁
１７　蛍光体
１８ａ，１８ｂ　絶縁層
１９　保護層
２０　画素
２１　シール部
３１，３２　維持パルス
３３　走査パルス
３４　データパルス
３５　消去パルス
３６　予備放電パルス
３７　予備放電消去パルス
３９　維持側共通パルス発生器
４０　走査側共通パルス発生器
４１，４２　維持パルス
５１　ＰチャンネルＦＥＴ
５２　ＮチャンネルＦＥＴ
５３　電解コンデンサ

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５４　　小容量のコンデンサ
６０　　維持パルス
６１，６２，６３，６４　　電圧の窪み
ＣＡ，ＣＢ，ＣＣ　　電極
ＤＤ１～ＤＤ１２　　ダイオード

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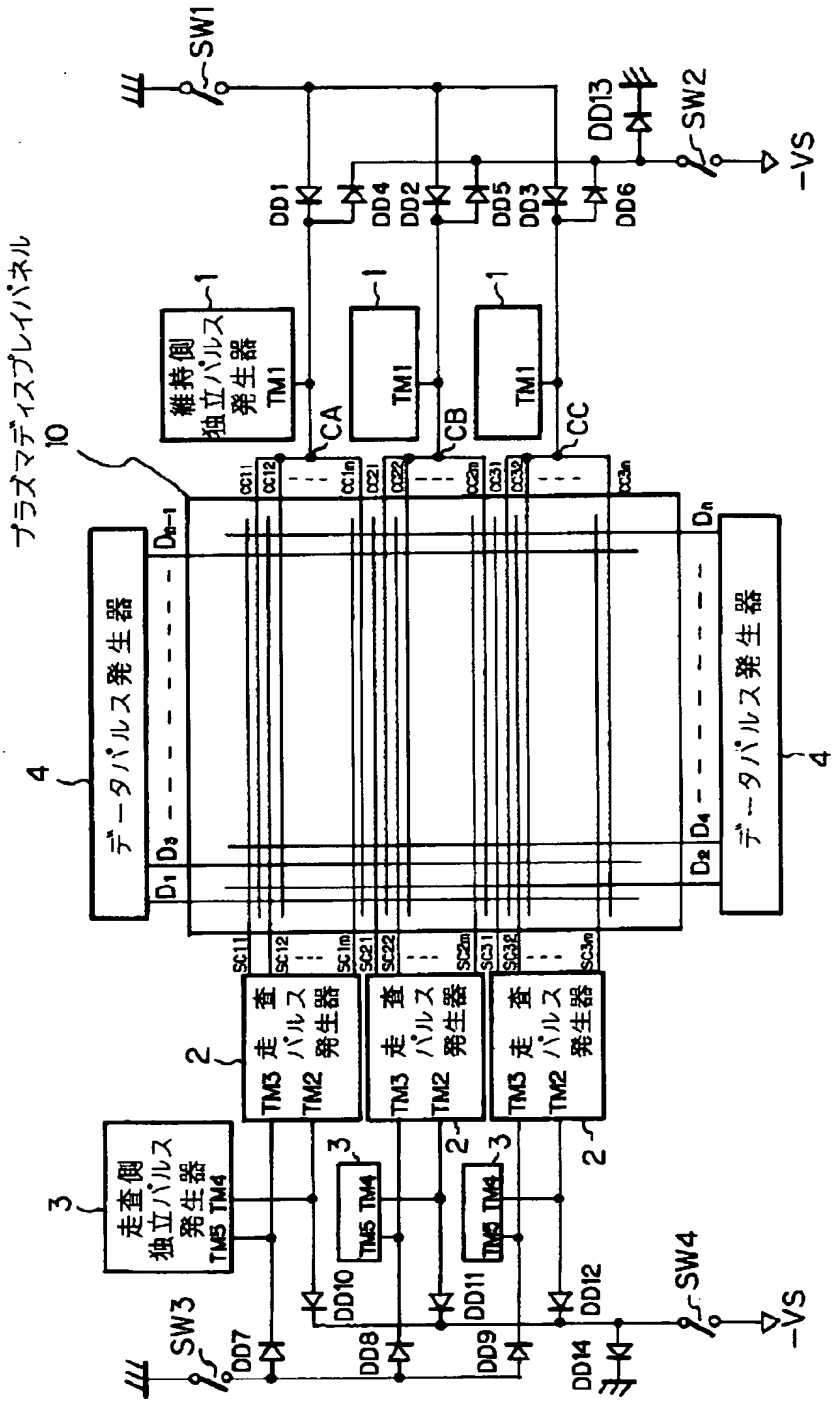
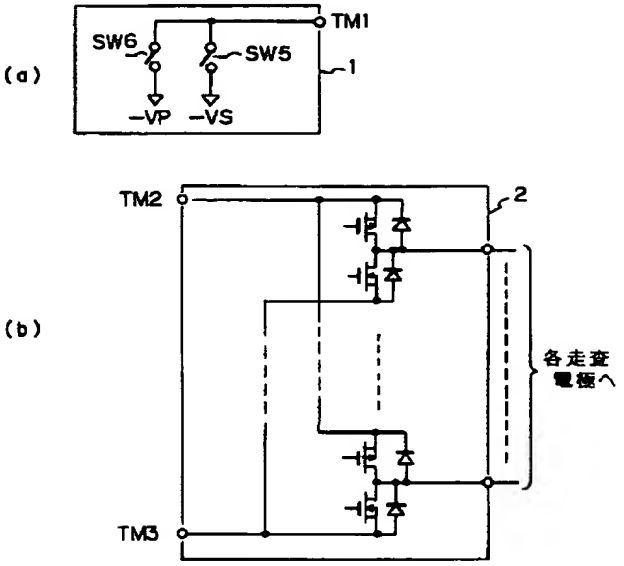
Ｇ，Ｈ，Ｉ　　走査電極ブロック
ＳＷ１～ＳＷ１１　　スイッチ
Ｌ１，Ｌ２　　コイル
ＰＰ１，ＰＰ２　　電圧測定ポイント

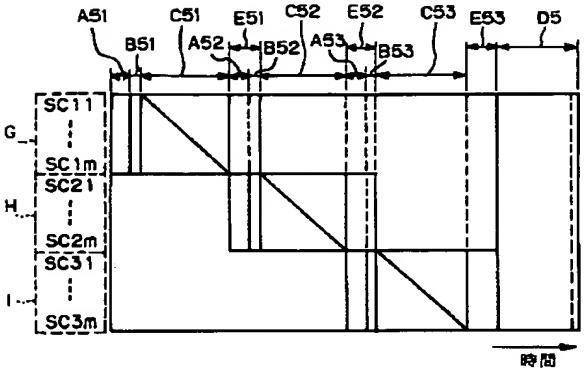
【図１】



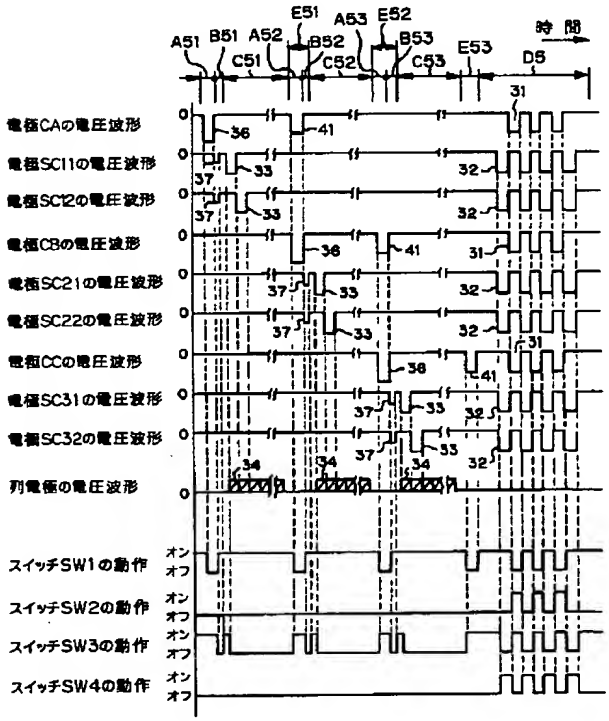
【図２】



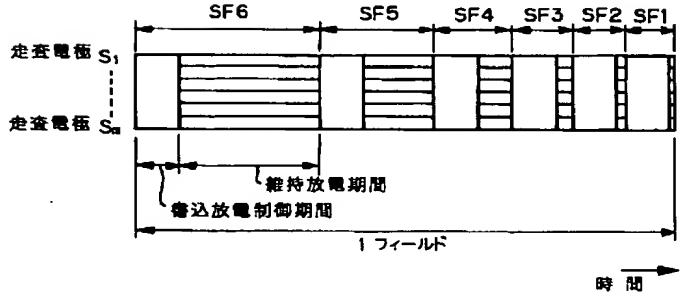
【図３】



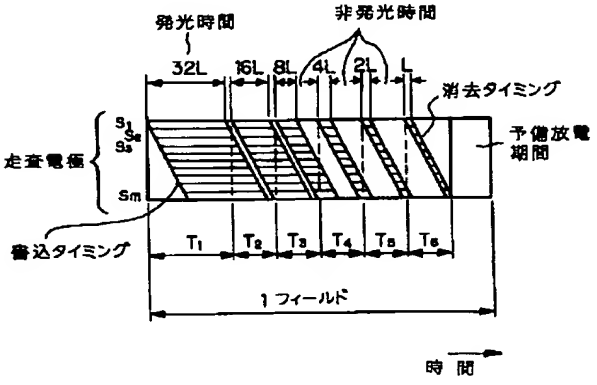
【図４】



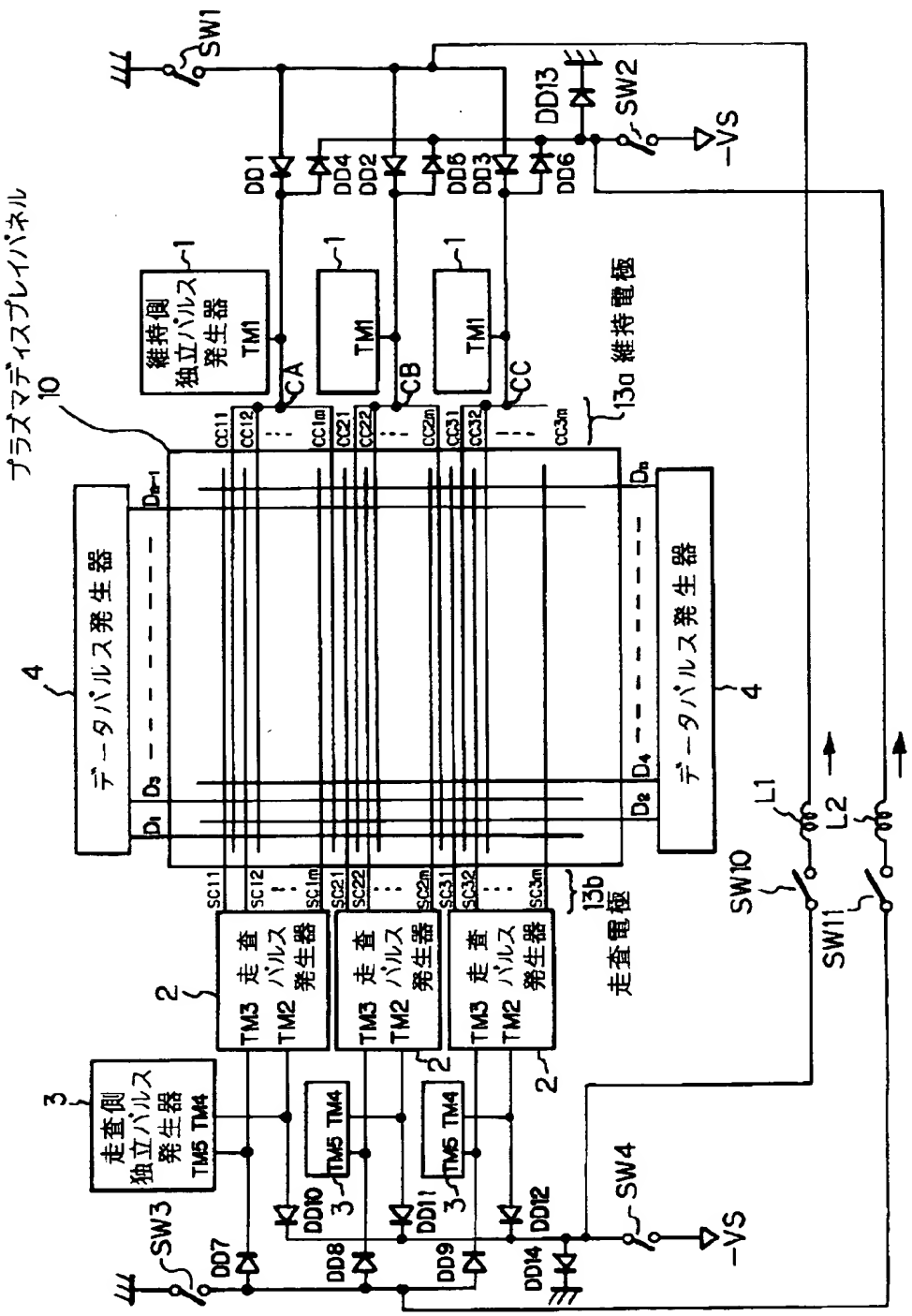
【図１０】



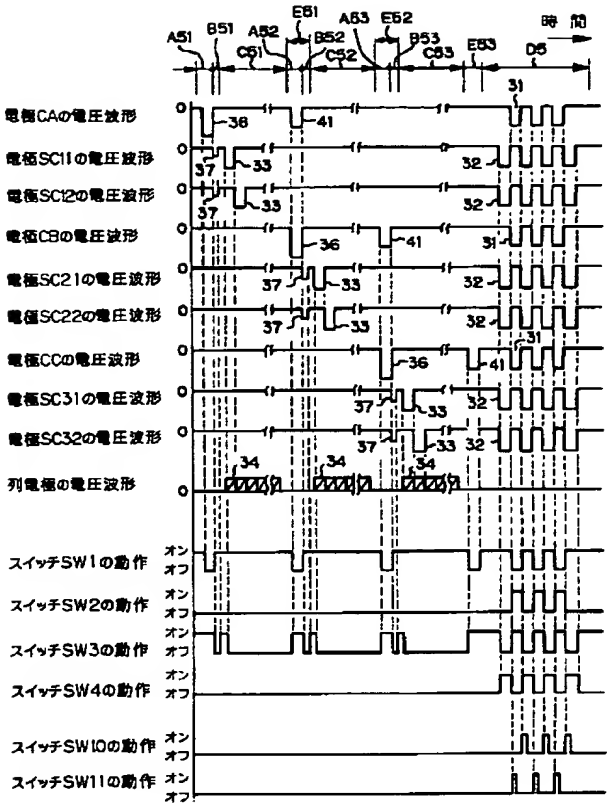
【図１２】



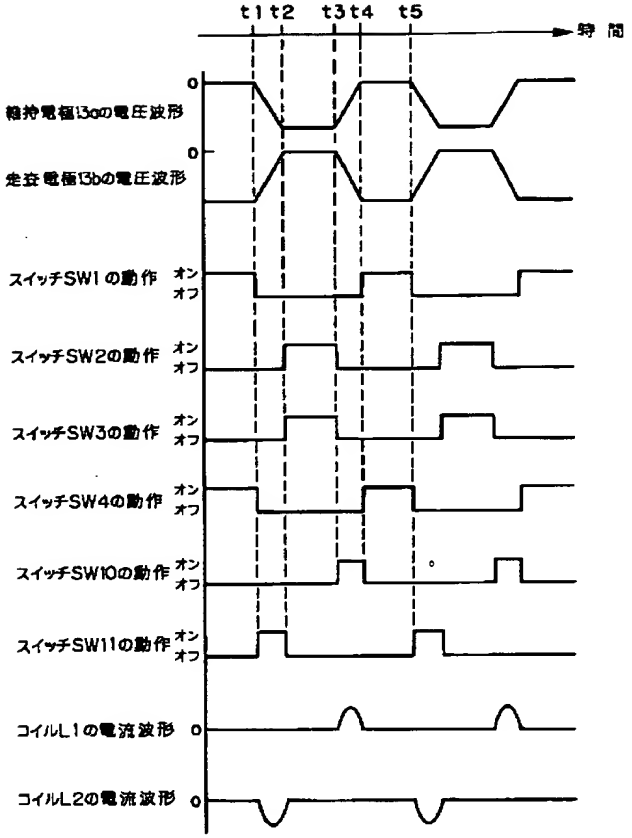
【図５】


プラズマディスプレイパネル
10
データパルス発生器
4
走査側独立パルス発生器
3
走査パルス発生器
2
維持側独立パルス発生器
1
TM1
TM2
TM3
TM4
TM5
SW1
SW2
SW3
SW4
SW10
SW11
L1
L2
-VS
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
CA
CB
CC
13a 維持電極
13b 走査電極

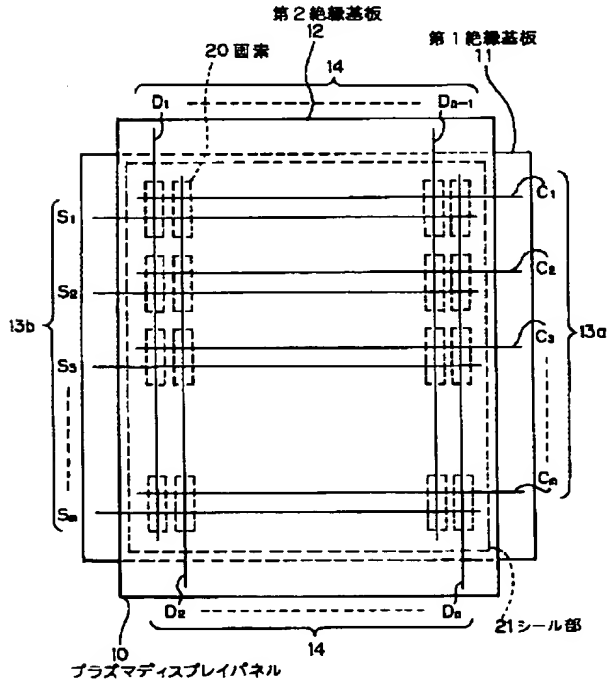
【図６】


A51
B51
A52
E61
B52
A53
E62
B53
E63
D5
時間
C61
C62
C63
電極CAの電圧波形
電極SC11の電圧波形
電極SC12の電圧波形
電極CBの電圧波形
電極SC21の電圧波形
電極SC22の電圧波形
電極CCの電圧波形
電極SC31の電圧波形
電極SC32の電圧波形
列電極の電圧波形
スイッチSW1の動作
スイッチSW2の動作
スイッチSW3の動作
スイッチSW4の動作
スイッチSW10の動作
スイッチSW11の動作
オン
オフ

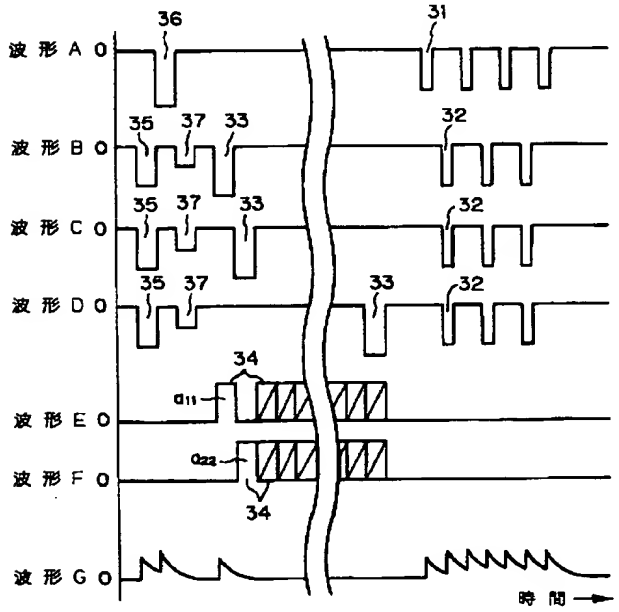
【図７】


t1 t2
t3 t4
t5
時間
維持電極13aの電圧波形
走査電極13bの電圧波形
スイッチSW1の動作
スイッチSW2の動作
スイッチSW3の動作
スイッチSW4の動作
スイッチSW10の動作
スイッチSW11の動作
コイルL1の電流波形
コイルL2の電流波形
オン
オフ

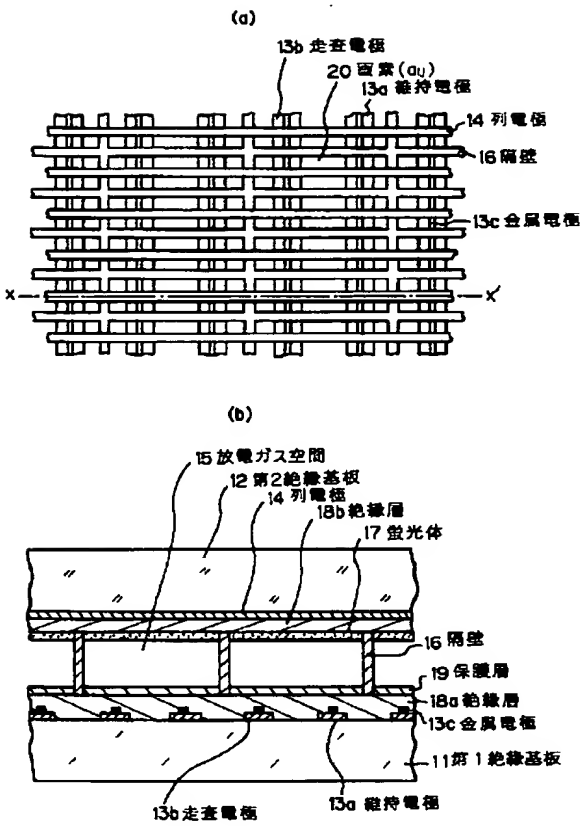
【図９】


第２絶縁基板
12
20 画素
第１絶縁基板
11
14
D1
Dn-1
C1
C2
C3
Cn
S1
S2
S3
Sm
13b
13a
D2
Dn
21 シール部
10
プラズマディスプレイパネル

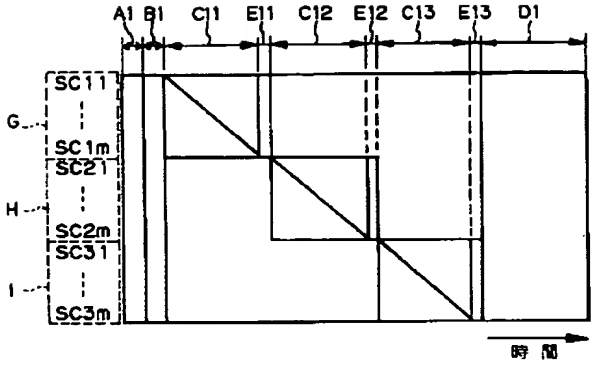
【図１１】


波形 A
波形 B
波形 C
波形 D
波形 E
波形 F
波形 G
時間

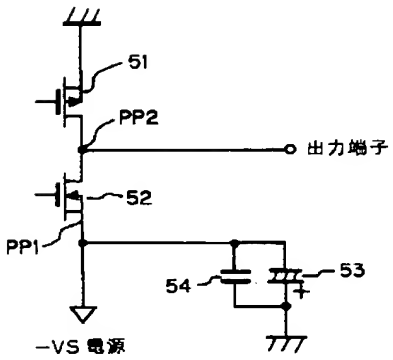
【図８】



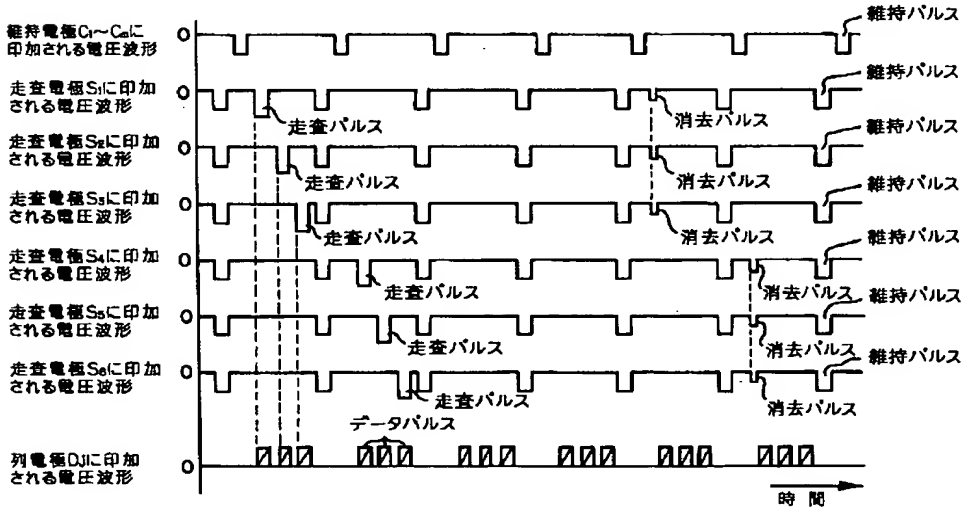
【図１４】



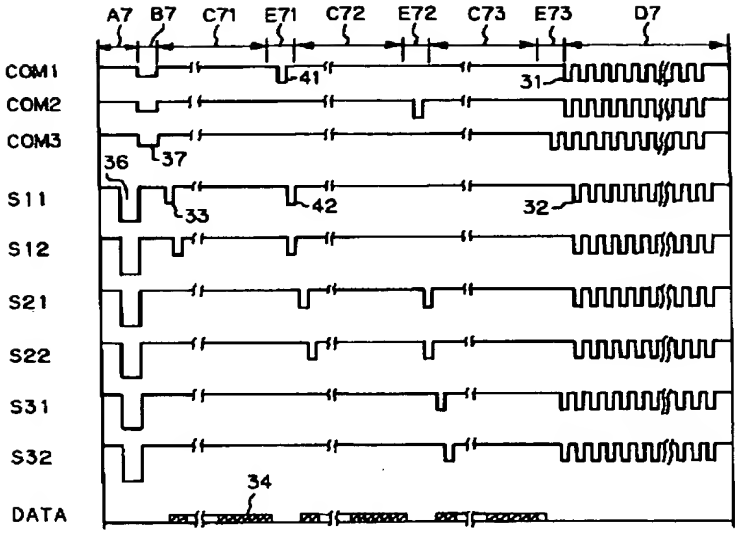
【図１７】



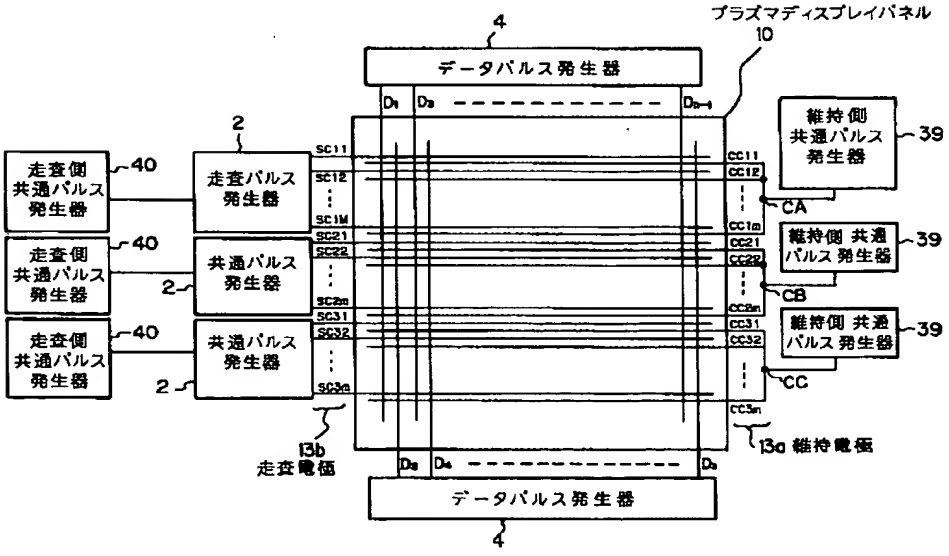
【図１３】



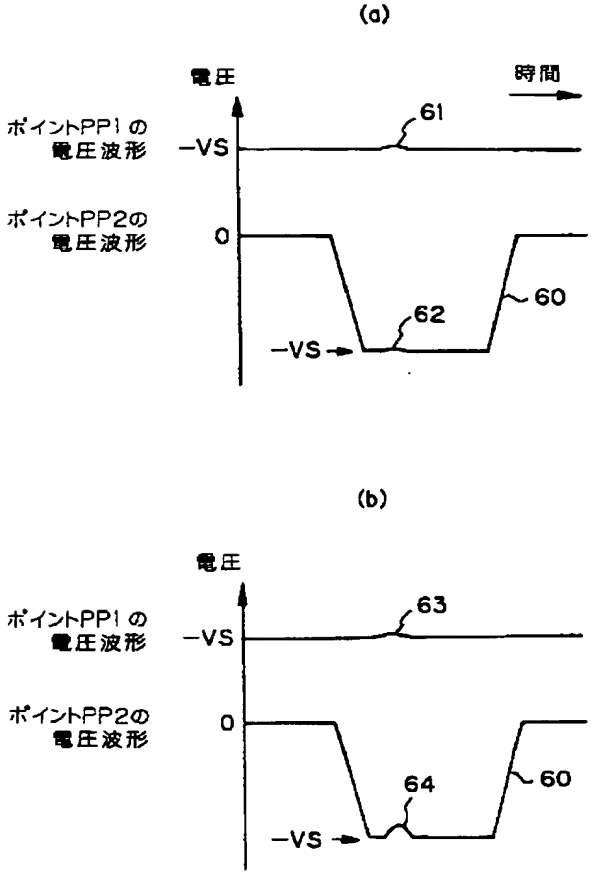
【図１５】


A7
B7
C71
E71
C72
E72
C73
E73
D7
COM1
COM2
COM3
S11
S12
S21
S22
S31
S32
DATA
41
31
36
37
33
42
32
34

【図１６】


4
データパルス発生器
プラズマディスプレイパネル
10
走査側
共通パルス
発生器
40
走査パルス
発生器
2
共通パルス
発生器
維持側
共通パルス
発生器
39
CA
CB
CC
13b
走査電極
13a 維持電極

【図１８】



フロントページの続き

(51) Int. Cl.[6]	識別記号	F I	
Ｇ０９Ｇ　3/20	６２４	Ｇ０９Ｇ　3/20	６２４Ｐ